PROFIBUS

User's manual

Version: **3.11 (September 2021)**
Order no.: **MAProfibus-ENG**

Translation of the original documentation

Publishing information

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1 Technical description

1.1 X20 bus controller

1.1.1 Order data

Order number	Short description	Figure
	Bus controllers	
X20BC0063	X20 bus controller, 1 PROFIBUS DP interface, 9-pin DSUB connection, order bus base, power supply module and terminal block separately	
	Required accessories	
	System modules for bus controllers	
X20BB80	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, X20 end cover plates (left and right) X20AC0SL1/X20AC0SR1 included	
X20PS9400	X20 power supply module, for bus controller and internal I/O power supply X2X Link power supply	
X20PS9402	X20 power supply module, for bus controller and internal I/O power supply, X2X Link power supply, supply not electrically isolated	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	
	Optional accessories	
	Infrastructure components	
0G1000.00-090	Bus connector, RS485, for PROFIBUS networks	

Table 1: X20BC0063 - Order data

1.1.2 Technical data

Order number	X20BC0063
Short description	
Bus controller	PROFIBUS DP V0 slave
General information	
B&R ID code	0x1F1C
Status indicators	Module status, bus function, data transfer
Diagnostics	
Module status	Yes, using status LED and software
Bus function	Yes, using status LED
Data transfer	Yes, using status LED
Power consumption	
Bus	2.3 W
Additional power dissipation caused by actuators (resistive) [W]	-
Certifications	
CE	Yes
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X
UL	cULus E115267 Industrial control equipment
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5
EAC	Yes
KC	Yes
Interfaces	
Fieldbus	PROFIBUS DP V0 slave
Variant	9-pin female DSUB connector
Max. distance	1200 m
Transfer rate	Max. 12 Mbit/s
Default transfer rate	Automatic transfer rate detection
Min. cycle time [1)]	
Fieldbus	No limitations
X2X Link	400 µs
Synchronization between bus systems possible	No

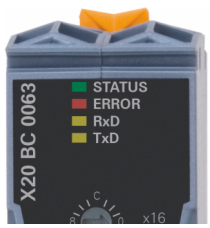
Table 2: X20BC0063 - Technical data

Order number	X20BC0063
Electrical properties	
Electrical isolation	PROFIBUS isolated from I/O PROFIBUS not isolated from bus
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation elevation above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
Degree of protection per EN 60529	IP20
Ambient conditions	
Temperature	
Operation	
Horizontal mounting orientation	-25 to 60°C
Vertical mounting orientation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical properties	
Note	Order 1x X20TB12 terminal block separately Order 1x X20PS9400 or X20PS9402 power supply module separately Order 1x X20BB80 bus base separately
Pitch [2]	37.5 $^{+0.2}$ mm

Table 2: X20BC0063 - Technical data

1) The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring.
2) Spacing is based on the width of the X20BB80 bus base. In addition, an X20PS9400 or X20PS9402 supply module is always required for the bus controller.

1.1.3 LED status indicators

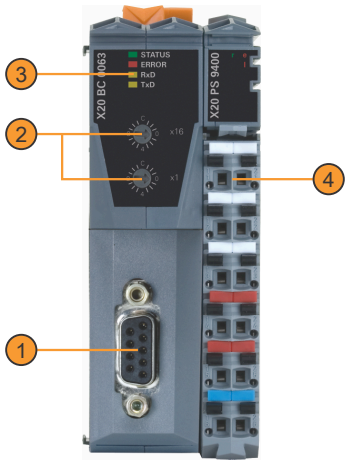
Figure	LED	Description		
	STATUS and ERROR	Status indicator for PROFIBUS DP bus controller.		
		STATUS (green)	**ERROR (red)**	**Description**
		Off	Off	HARDWARE FAULT / POWER FAIL
		On	On	BUS OFF
		On	Blinking	WAIT FOR CONFIG
		Blinking	Off	DATA EXCHANGE - DIAGNOSTICS
		On	Off	DATA EXCHANGE - NO ERROR
		Blinking	Blinking	CONFIG ERROR
		Off	Blinking	SERVICE MODE - BOOT
		Single flash	Single flash	HARDWARE FAULT
		For a more detailed description see "State diagnostics via the Status/Error LEDs" on page 9.		
	RxD	This yellow LED lights up when the bus controller is receiving data from the PROFIBUS DP fieldbus.		
	TxD	This yellow LED lights up when the bus controller is sending data via the PROFIBUS DP fieldbus.		

1.1.3.1 State diagnostics via the Status/Error LEDs

The condition of the PROFIBUS DP bus controller is diagnosed using the LED status indicators "STATUS" and "ERROR".

STATUS (green)	ERROR (red)	Function	Solution
Off	Off	HARDWARE FAULT / POWER FAILURE	• Check wiring of supply voltage.
On	On	BUS OFF • Baud rate not detected • No connection to the DP master • DP master not active	• Check the PROFIBUS network • Check the PROFIBUS master
On	Blinking	WAIT FOR CONFIG • Transfer rate has been detected, but the PROFIBUS master has not yet configured the bus controller	• Check the node number switch • Check the slave address in the master configuration
Blinking	Off	DATA EXCHANGE - DIAGNOSTICS • The bus controller is still initializing the I/O modules • The I/O modules configured by the master cannot be found • An error has occurred on one or more I/O modules (short circuit, etc.)	• Initialization can take a few seconds depending on the number of I/O modules connected • Check the wiring and power supply for the I/O modules • Read diagnostic messages in the respective PROFIBUS master's engineering tool
On	Off	DATA EXCHANGE • Cyclic data exchange with the PROFIBUS DP master	
Blinking	Blinking	CONFIG ERROR • One or more I/O modules found do not match with the configuration of the PROFIBUS DP master • The configuration received from the PROFIBUS master is invalid	• Check the wiring of the X2X Link and the order of I/O modules • Check configuration of the PROFIBUS master • Read diagnostic messages in the respective PROFIBUS master's engineering tool • Check the configuration being used - it is possible that the number of configured I/O modules is too high
Off	Blinking	SERVICE MODE - BOOT • The bus controller's node number has been set to 255 (0xFF) - after 2 s the bus controller starts in service mode	• Set a valid node number
Single flash	Single flash	HARDWARE FAULT	

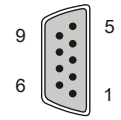
1.1.4 Operating and connection elements



1	PROFIBUS DP connection	2	Node number switches
3	LED status indicators	4	Terminal block for bus controller and I/O supply

1.1.4.1 PROFIBUS DP interface

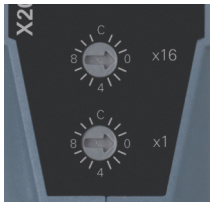
A shielded line must be used for the interface.

Interface	Pinout		
 9-pin female DSUB connector	**Pin**	**RS485**	
	1	Reserved	
	2	Reserved	
	3	RxD/TxD-P	Data[1]
	4	CNTR-P	Transmit enable
	5	DGND	Power supply
	6	VP	Power supply
	7	Reserved	
	8	RxD/TxD-N	Data\[2]
	9	CNTR-N	Transmit enable\
	CNTR ... Direction switch for external repeaters		

1) Cable color: Red
2) Cable color: Green

1.1.4.2 PROFIBUS DP node number switches

The PROFIBUS DP node number is configured using both number switches of the bus controller.



Switch position	Node number
0x00	Not allowed
0x01 - 0x7D	1 to 125
0x7E - 0xFF	Not allowed

1.1.4.3 Automatic transfer rate detection

After booting or after a communication timeout, the bus controller goes into the status "Baud Search". This means the bus controller behaves passively on the bus.

The bus controller always begins the search for the configured transfer rate with the highest transfer rate. If a complete error-free telegram is not received during monitoring time, then the search is continued using the next lowest transfer rate.

Transfer rate
12 Mbit/s
6 Mbit/s
3 Mbit/s
1.5 Mbit/s
500 kbit/s
187.5 kbit/s
93.75 kbit/s
45.45 kbit/s
19.2 kbit/s
9.6 kbit/s

1.2 X67 bus controller

1.2.1 Order data

Order number	Short description	Figure
	Bus controller modules	
X67BC6321	X67 bus controller, 1 PROFIBUS DP interface, X2X Link power supply 3 W, 8 digital channels configurable as inputs or outputs, 24 VDC, 0.5 A, configurable input filter, 2 event counters 50 kHz	
X67BC6321.L08	X67 bus controller, 1 PROFIBUS DP interface, X2X Link power supply 15 W, 16 digital channels configurable as inputs or outputs, 24 VDC, 0.5 A, configurable input filter, 2 event counters 50 kHz, M8 connectors, high-density module	
X67BC6321.L12	X67 bus controller, 1 PROFIBUS DP interface, X2X Link power supply 15 W, 16 digital channels configurable as inputs or outputs, 24 VDC, 0.5 A, configurable input filter, 2 event counters 50 kHz, M12 connectors, high-density module	

Table 3: X67BC6321, X67BC6321.L08, X67BC6321.L12 - Order data

1.2.2 Technical data

Order number	X67BC6321	X67BC6321.L08	X67BC6321.L12
Short description			
Bus controller	PROFIBUS DP V0		
General information			
Inputs/Outputs	8 digital channels, configurable as inputs or outputs using software, inputs with additional functions	16 digital channels, configurable as inputs or outputs using software, inputs with additional functions	
Insulation voltage between channel and bus	500 V_{Eff}		
Nominal voltage	24 VDC		
B&R ID code			
Bus controller	0x1436	0x1AEB	0x1AEC
Internal I/O module	0x1311	0x1A1C	0x1A1D
Sensor/Actuator power supply	0.5 A summation current		
Status indicators	I/O function for each channel, supply voltage, bus function		
Diagnostics			
Outputs	Yes, using status LED and software		
I/O power supply	Yes, using status LED and software		
Connection type			
Fieldbus	M12, B-keyed		
X2X Link	M12, B-keyed		
Inputs/Outputs	8x M8, 3-pin	16x M8, 3-pin	8x M12, A-keyed
I/O power supply	M8, 4-pin		
Power output	3 W X2X Link power supply for I/O modules	15 W X2X Link supply for I/O modules	
Power consumption			
Fieldbus	3.8 W	3.25 W	
Internal I/O	2 W	2.04 W	
X2X Link power supply	7.5 W at maximum power output for connected I/O modules	23.63 W at maximum power output for connected I/O modules	
Certifications			
CE	Yes		
ATEX	Zone 2, II 3G Ex nA IIA T5 Gc IP67, Ta = 0 - Max. 60°C TÜV 05 ATEX 7201X		
UL	cULus E115267 Industrial control equipment		
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5		
EAC	Yes		
KC	Yes		
Interfaces			
Fieldbus	PROFIBUS DP V0		
Variant	M12 interface (female connector on module)	2x M12 interface for the Y-connector integrated in the module	
Max. distance	1200 m		
Transfer rate	Max. 12 Mbit/s		

Table 4: X67BC6321, X67BC6321.L08, X67BC6321.L12 - Technical data

Order number	X67BC6321	X67BC6321.L08	X67BC6321.L12
Default transfer rate	Automatic transfer rate detection		
Min. cycle time [1]			
Fieldbus	No limitations		
X2X Link	400 µs		
Synchronization between bus systems possible	No		
PROFIBUS DP ID	0x6321	0xBC60	0xBC61
Terminating resistor	Can be optionally screwed onto the Y-connector	Can be optionally screwed onto the integrated Y-connector	
I/O power supply			
Nominal voltage	24 VDC		
Voltage range	18 to 30 VDC		
Integrated protection	Reverse polarity protection		
Power consumption			
Sensor/Actuator power supply	Max. 12 W [2]		
Sensor/Actuator power supply			
Voltage	I/O power supply minus voltage drop for short circuit protection		
Voltage drop for short-circuit protection at 0.5 A	Max. 2 VDC		
Summation current	Max. 0.5 A		
Short-circuit proof	Yes		
Digital inputs			
Input characteristics per EN 61131-2	Type 1		
Input voltage	18 to 30 VDC		
Input current at 24 VDC	Typ. 4 mA		
Input circuit	Sink		
Input filter			
Hardware	≤10 µs (channels 1 to 4) / ≤70 µs (channels 5 to 8)	≤10 µs (channels 1 to 4) / ≤70 µs (channels 5 to 16)	
Software	Default 0 ms, configurable between 0 and 25 ms in 0.2 ms intervals		
Input resistance	Typ. 6 kΩ		
Additional functions	50 kHz event counting, gate measurement		
Switching threshold			
Low	<5 VDC		
High	>15 VDC		
Event counters			
Quantity	2		
Signal form	Square wave pulse		
Evaluation	Each falling edge, cyclic counter		
Input frequency	Max. 50 kHz		
Counter 1	Input 1		
Counter 2	Input 3		
Counter frequency	Max. 50 kHz		
Counter size	16-bit		
Gate measurement			
Quantity	1		
Signal form	Square wave pulse		
Evaluation	Rising edge - Falling edge		
Counter frequency			
Internal	48 MHz, 3 MHz, 187.5 kHz		
Counter size	16-bit		
Length of pause between pulses	≥100 µs		
Pulse length	≥20 µs		
Supported inputs	Input 2 or input 4		
Digital outputs			
Variant	FET positive switching		
Switching voltage	I/O power supply minus residual voltage		
Nominal output current	0.5 A		
Total nominal current	4 A	8 A	
Output circuit	Source		
Output protection	Thermal cutoff for overcurrent and short circuit, integrated protection for switching inductances, reverse polarity protection for output power supply		
Diagnostic status	Output monitoring with 10 ms delay		
Leakage current when the output is switched off	5 µA		
Switching on after overload shutdown	Approx. 10 ms (depends on the module temperature)		
Residual voltage	<0.3 V at 0.5 A rated current		
Peak short-circuit current	<12 A		
Switching delay			
0 → 1	<400 µs		
1 → 0	<400 µs		
Switching frequency			
Resistive load	Max. 100 Hz		
Inductive load	See section "Switching inductive loads"		
Braking voltage when switching off inductive loads	50 VDC		

Table 4: X67BC6321, X67BC6321.L08, X67BC6321.L12 - Technical data

Order number	X67BC6321	X67BC6321.L08	X67BC6321.L12
Electrical properties			
Electrical isolation	Channel isolated from PROFIBUS and bus PROFIBUS not isolated from bus and channel not isolated from channel		
Operating conditions			
Mounting orientation			
Any	Yes		
Installation elevation above sea level			
0 to 2000 m	No limitations		
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m		
Degree of protection per EN 60529	IP67		
Ambient conditions			
Temperature			
Operation	-25 to 60°C		
Derating	-		
Storage	-40 to 85°C		
Transport	-40 to 85°C		
Mechanical properties			
Dimensions			
Width	53 mm		
Height	85 mm	155 mm	
Depth	42 mm		
Weight	200 g	355 g	375 g
Torque for connections			
M8	Max. 0.4 Nm		
M12	Max. 0.6 Nm		

Table 4: X67BC6321, X67BC6321.L08, X67BC6321.L12 - Technical data

1) The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring.
2) The power consumption of the sensors and actuators connected to the module is not permitted to exceed 12 W.

1.2.3 LED status indicators

The bus controller is equipped with one Link LED that indicates the current "Ethernet" link status or activity on both ports.

Figure	LED	Color	Status	Description
	**Status indicator 1**: Status indicator for Modbus TCP bus controller			
	L/A IF (Link/Active)	Green	Blinking	The LED blinks when there is Ethernet activity on the Ethernet interface.
			Permanently on	Connection (link) established on the Ethernet connection, however there is no communication.
			Off	Indicates that no physical Ethernet connection exists
	S/E[1] (Status/Error)	Green	Permanently on	Indicates that there is at least one client connection
			2 pulses	Indicates that there are no client connections
			4 pulses	Indicates that the controller is waiting for an address from the DHCP server
			Blinking	Initialization of connected I/O modules
		Red	Permanently on	Indicates a major unrecoverable hardware fault
			2 pulses	Watchdog timeout
			3 pulses	Faulty I/O module configuration data
			4 pulses	Indicates that the controller has detected an IP address being used twice
			5 pulses	Indicates a missing, defective or incorrect I/O module
			6 pulses	Error reading from or writing to flash memory
	I/O LEDs			
	1 - 8	Orange	-	Input/Output status of the corresponding channel
	Status indicator 2: Status indicator for module functionality			
	Left	Green	Off	No power to module
			Single flash	Mode RESET
			Blinking	Mode PREOPERATIONAL
			On	Mode RUN
	Right	Red	Off	Module not supplied with power or everything OK
			On	Error or reset state
			Single flash	Warning/Error on an I/O channel. Level monitoring for digital outputs has been triggered.
			Double flash	Supply voltage not in the valid range

1) This LED is a green/red dual LED. Several red blinking signals are displayed immediately after the device is switched on. These are startup messages, however, and not errors.

The status/error LED is a green and red dual LED. The color green (status) is superimposed on the color red (error).

Information:

Several red blinking signals are displayed immediately after the device is switched on. These are start-up messages, however, and not errors.

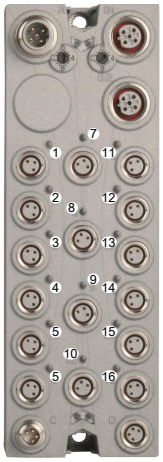
Status/Error LED lit red: Error state indication

Red - Error	Description
2 pulses	Watchdog timeout
3 pulses	Faulty I/O module configuration data
4 pulses	Indicates that the controller has detected an IP address being used twice
5 pulses	Indicates a missing, defective or incorrect I/O module
6 pulses	Error reading from or writing to flash memory
Permanently red	Indicates a major unrecoverable fault

Status/Error LED lit green: Operating state indication

Green - Status	Description
Permanently green	Indicates that there is at least one client connection
2 pulses	Indicates that there are no client connections
4 pulses	Indicates that the controller is waiting for an address from the DHCP server
Blinking	Initialization of connected I/O modules

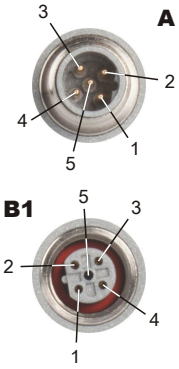
1.2.4 Operating and connection elements



1.2.4.1 PROFIBUS DP interface

The bus controller is connected to the fieldbus using pre-assembled cables. The connection is made using M12 circular connectors.

The Y-connector for PROFIBUS DP is already integrated in this module.

Connection	Pinout			
	**Pin**	**PROFIBUS DP**		
	1	+5 V[1)]	-	-	-
	2	A	RxD/TxD-N	Data\	Green
	3	GND[1)]	-	-	-
	4	B	RxD/TxD-P	Data	Red
	5	Shield[1)]	-	-	-
	1) Shield connection also made via threaded insert in the module A → B-keyed (male), input B1 → B-keyed (female), output			

1) Supply for terminating resistor (PROFIBUS DP standard) generated internally by the bus controller. These pins are irrelevant for wiring.

1.2.4.2 PROFIBUS DP node number

The PROFIBUS DP node number is configured using both number switches of the bus controller.

Node number 0xFF enables service mode. Modus. The bus controller starts with PROFIBUS DP address 2. A firmware update is possible in service mode. The I/Os cannot be operated.



1.2.4.3 Automatic transfer rate detection

After booting or after a communication timeout, the bus controller goes into the status "Baud Search". This means the bus controller behaves passively on the bus.

The bus controller always begins the search for the configured transfer rate with the highest transfer rate. If a complete error-free telegram is not received during monitoring time, then the search is continued using the next lowest transfer rate.

Transfer rate
12 Mbit/s
6 Mbit/s
3 Mbit/s
1.5 Mbit/s
500 kbit/s
187.5 kbit/s
93.75 kbit/s
45.45 kbit/s
19.2 kbit/s
9.6 kbit/s

1.3 Firmware installed prior to delivery

X20BC0063

Hardware revision (see label on the module)	Firmware version	Comment
A1	1.27	
A2	1.29	
A3	1.31	
B0, C0	1.40	
D0	1.44	Certification
E0, F0	1.45	
G0, H0, I0	1.47	

X67BC6321

Hardware revision (see label on the module)	Firmware version	Comment
A0	1.23	
F0, G0, H0	1.25	Support for X20 I/O modules
K0	1.48	

X67BC6321.L08

Hardware revision (see label on the module)	Firmware version	Comment
A0	1.26	
A2, A3, A5, C0, D0, E0, F0, G0	1.29	
H0	1.43	
I0, J0	1.44	Certification
K0, L0	1.45	
M0	1.47	
N0	1.48	

X67BC6321.L12

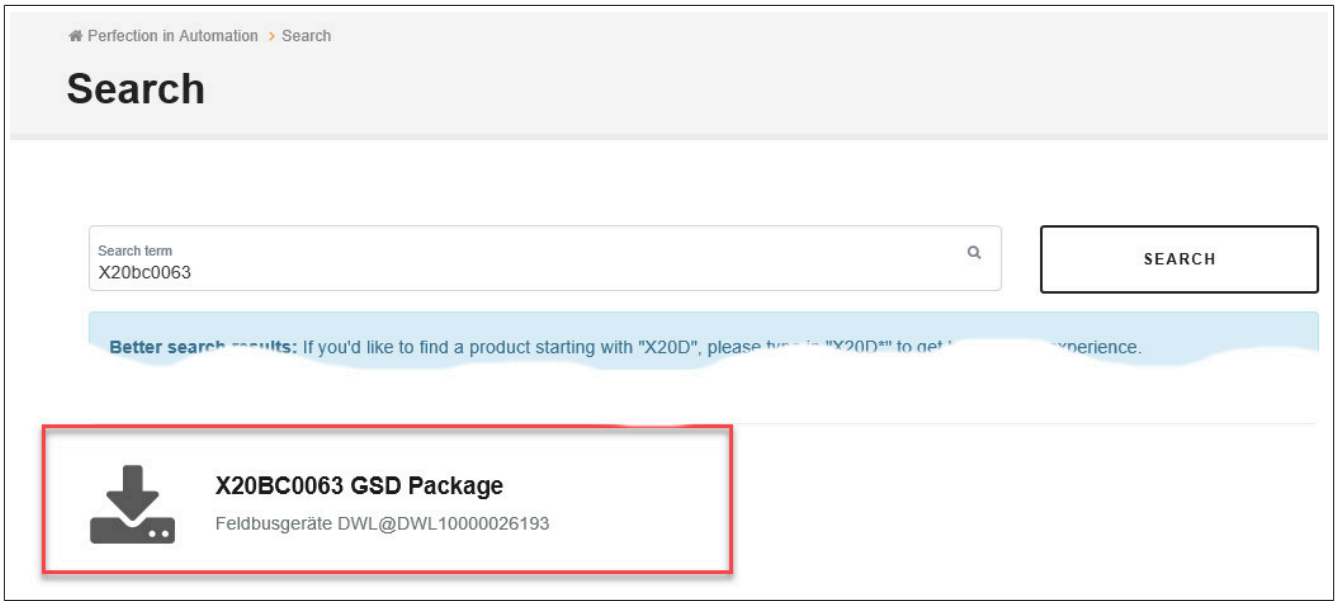
Hardware revision (see label on the module)	Firmware version	Comment
A0	1.26	
AA, B0, C0, D0, E0	1.30	
F0	1.43	
G0	1.44	Certification
I0, H0	1.45	
J0	1.47	
L0, K0, M0	1.48	

2 Installation

Importing the appropriate general station description file (GSD file) is required for successfully integrating the B&R PROFIBUS DP bus controller in an engineering tool. This is available on the B&R website (www.br-automation.com) for all PROFIBUS DP bus controllers. The corresponding product information appears by specifying the product or serial number in the product search. The Downloads section for each module has a link to the GSD package. In addition to various graphics files, this includes the PROFIBUS user's manual, the "B&R BC PROFIBUS Design Tool" and the required GSD file.

A version number can be selected before downloading the file. The highest available version should be used when integrating a PROFIBUS controller in an engineering tool for the first time.

It is not necessary to update previously integrated GSD files, since using a newer GSD file might require the latest firmware. A firmware update cannot be performed by the user. After unpacking the compressed file, the GSD file is located in folder "Import".



2.1 GSD file

Filename:

B&R_6321.GSD for X67BC6321 (Device ID 0x6321)
B&R_BC60.GSD for X67BC6321.L08 (Device ID 0xBC60)
B&R_BC60.GSD for X67BC6321.L08 (Device ID 0xBC60)
B&R_BC20.GSD for X20BC0063 (Device ID 0xBC20)

The GSD file must be imported in the master system's engineering tool in order to use the bus controller.

Example: Siemens STEP 7 V 5.1

- Open the hardware configuration (HW Config)
- Select "Tools → Install new GSD..." from the menu
- Select the GSD file

2.2 Bitmaps

Two bitmaps (.DIB) are delivered together with the GSD file. They are used to display the current state of the individual bus controllers in the engineering tool.

Example: Siemens STEP 7 V 5.1

- When the GSD file is imported, the bitmaps must be stored in the same directory.

3 Configuration

The B&R BC PROFIBUS Design Tool makes it possible to test the desired bus configuration feasibility. After selecting the bus controller used, local I/O and X2X cycle time, all conceivable variants of the connected I/O modules can be configured. If the combination entered is technically feasible, status display "Ok" appears. The total number of modules selected is listed in parentheses. The bus controller itself is counted automatically, so at least 1 module is always configured. If there are conflicts in the configuration, the status indicator reads "Parameter frame too big (PROFIBUS DP standard)".

Various times in the range of 200 µs to 1 ms are available for selection in input field X2X cycle time. The desired number of I/O modules can be entered in the gray column "Used".

The configuration sequence of I/O modules on the bus is irrelevant here; only performance-related data is relevant. X67 system supply modules (X67PS1300) cannot be configured since they do not have I/O data traffic in their function as pure electronic modules for power supply. All other modules require an entry. To make the configuration process as simple as possible, column "Available" lists the maximum possible number of each module. This is dynamic and automatically updated after every entry.

When selecting the X20 bus controller, the only local I/O available is the necessary X20PS9400. Multiple variants of the X67 bus controllers can be selected as Local I/Os however. They are identified by extension "-CO1, -CO2,..." at the end of their name. This describes the respective register assignment in the module (see respective register description). If no selection is made, the value suggested by the design tool can be used.

The following figure shows a section of the B&R BC PROFIBUS Design Tool.

B&R BC Profibus Design Tool V2.18

Status	Ok (15 modules configured).
Profibus Controller:	X20BC0063
Local IO:	X20 PS 9400
X2X Cycle Time:	1 ms

X2X Modules:

Type	Info	Used	Available
X20 AI 2622: 2 AI, 12 Bit	cyclic:data	1	13
X20 AI 2632: 2 AI, 16 Bit	cyclic:data	2	8
X20 AI 4622: 4 AI, 12 Bit	cyclic:data		13
X20 AI 4632: 4 AI, 16 Bit	cyclic:data	3	6

X20 AO 2622: 2 AO, 12 Bit	cyclic:data	1	21
X20 AO 2632: 2 AO, 16 Bit	cyclic:data		15
X20 AO 4622: 4 AO, 12 Bit	cyclic:data	5	21
X20 AO 4632: 4 AO, 16 Bit	cyclic:data		13

X20 AT 2222: 2 Temperature	cyclic:data+diag		13
X20 AT 2402: 2 Termocouple	cyclic:data+diag		15
X20 AT 4222: 4 Temperature	cyclic:data+diag		11
X20 AT 6402: 6 Termocouple	cyclic:data+diag		14

X20 BR 9300: Bus Receiver	cyclic:data	1	26
X20 BT 9100: Bus Transmitter	cyclic:data	1	26

3.1 Configuring the I/O modules

The I/O module can be configured either via the cyclic PROFIBUS data or using dialog boxes in the engineering tool.

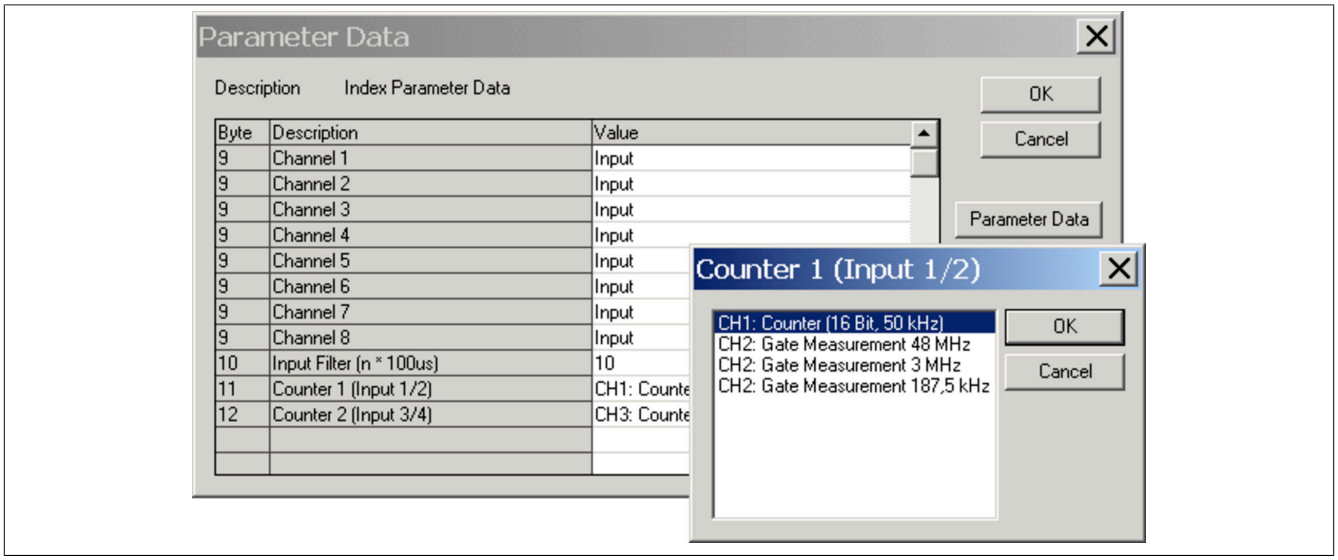
Information:

On bus controllers with an integrated I/O module, the first slot must be used for this module:

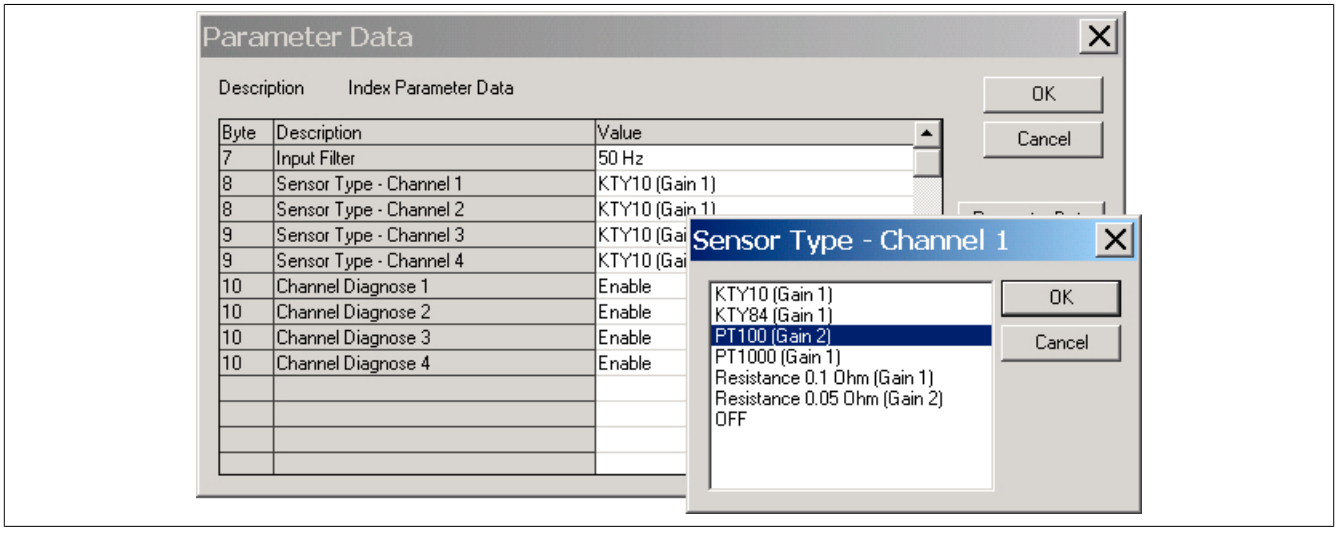
X20BC0063	**No integrated I/O module**
X67BC6321	**X67DM1321**
X67BC6321.L08	**X67DM1321.L08**
X67BC6321.L12	**X67DM1321.L12**

Examples of parameter dialog boxes

Configuration (X67DM1321-C21)



Configuration (X67AT1322-C01)



3.2 Configuring the bus controller

The bus controller parameters below can be modified with the dialog boxes in the engineering tool.

The "Value" column refers to the coding of the parameters in the parameter telegram.

3.2.1 Data format

Selection	Value	Description
Big Endian (default)	0	Registers which have a size > 1 byte in the register description are transferred in Big Endian format (high byte first) (PROFIBUS DP standard).
Little Endian	1	Registers > 1 byte are transferred in Little Endian format. This function can be used when the master system is a Little Endian system. If the PROFIBUS DP master also supports this functionality, the user must make sure that conversion takes place either only on the master or only on the slave.

3.2.2 Slot diagnostics

Selection	Value	Description
DP Standard (default)	0	PROFIBUS DP slot diagnostics are not enabled. **Reason:** This diagnostic information is interpreted differently by different master systems. This may cause diagnostic messages to not show slot numbers (module numbers) correctly. In order to display the corresponding information correctly on all master systems, the slot diagnostic data is transferred in bytes 12 to 19 in the diagnostic telegram instead. (See "Structure of the diagnostics telegram" on page 28.)
S7 format	1	Advanced slot diagnostics for S7 systems. With other master systems that function strictly according to the PROFIBUS DP standard, this setting can cause the slot numbers to be displayed incorrectly.

3.2.3 Bus controller behavior for missing modules

The setting "Behavior for missing modules“determines the behavior of the bus controller if configured modules are missing from the current configuration.

Selection	Value	Description
Extended diagnostics	0	The bus controller reports missing I/O modules with extended diagnostics. The existing I/O modules can still be operated.
Static diagnostics	1	A static diagnostics report is provided to the master. The outputs are set to the defaults and cannot be operated. However, this only applies to I/O modules that are not detected when booting. If I/O modules drop out while the bus controller is exchanging data, starting extended diagnostics is the only action taken.
No diagnostics	2	Diagnostics is not generated for missing modules, the use must actively use the PROFIBUS service GetConfig to ask which I/O modules are actually available. Removing/adding I/O modules on a bus controller while it is exchanging data still results in various diagnostics messages being created, because this can cause short disturbances on the I/O bus.

(The setting is only evaluated starting with firmware version 1.32 on the bus controller.)

3.2.4 Supply voltage warnings

Setting "Supply voltage warnings" defines whether or not the bus controller sends supply voltage warning messages (PROFIBUS DP diagnostic message, see "Structure of the diagnostics telegram" on page 28) to the master.

Selection	Value	Description
Enable	0 (default)	The bus controller sends supply voltage alarms to the master.
Disable	1	NO supply voltage alarms are sent. The PROFIBUS DP diagnostics messages are not sent by the bus controller, which means they aren't available on the PROFIBUS DP network. The LED status indicators for the X2X modules and the bus controller show very clearly that there is a problem with the supply voltage, however.

(The setting is only evaluated starting with firmware version 1.47 on the bus controller.)

3.2.5 X2X cycle time

Selection	Value	Description
1 ms (default)	0	The "X2X cycle time" parameter configures the I/O cycle time on the X2X Link.
900 µs	1	
800 µs	2	
700 µs	3	
600 µs	4	
500 µs	5	
400 µs	6	

Information:

Information: Short bus cycles reduce the maximum number of I/O modules possible on the X2X Link network (see "B&R BC PROFIBUS Design Tool" on the B&R website www.br-automation.com).

3.2.6 Slowest I/O modules

This setting allows I/O modules to be used which are not able to communicate in each X2X Link cycle.

Example

The X2X cycle time is set to 400 µs in order to scan a digital input as fast as possible. In the same system, another module should also be used that does not support this cycle time (see documentation for the respective I/O module).

This setting should normally always be left at its default. Other values result in the system requiring much longer to be initialized.

Selection	Value	Description
1 X2X cycle (default)	0	Each connected I/O module must supply valid data in every X2X cycle. If there are modules on the X2X bus for which the configured X2X cycle is too short, an error is reported on the master.
2 X2X cycles	1	Each connected I/O module must supply valid data in every 2nd X2X Link cycle.
3 X2X cycles	2	Each connected I/O module must supply valid data in every 3rd X2X Link cycle.
...		...
8 X2X cycles	7	Each connected I/O module must supply valid data in every 8th X2X Link cycle.

3.3 Structure of the PROFIBUS DP parameter telegram

The parameter telegram is automatically transferred from the master to the bus controller when the connection is established.

Byte	Description
0 - 6	See "PROFIBUS DP standard DIN 19245-3" (the parameters in these bytes are automatically generated by the Engineering Tool)
7	Protocol parameters
8	Parameter flag 1
9	Parameter flag 2
10	Whole number portion of the minimum firmware version required (must not be modified by the user)
11	Decimal portion of the minimum firmware version required (must not be modified by the user). (Bytes 10 and 11 tell the bus controller the minimum firmware version required for this GSD file.)
12	Number of expansion parameter bytes (for future expansions)
...	Parameter data for the configured I/O modules then follows. This data is automatically generated by the engineering tool and is only permitted to be changed using the module parameter dialog boxes (see "Configuring the I/O modules" on page 20).

Protocol parameters

Bit	Description	Value
0 - 2	Internal	0
3 - 4	Reserved	0
5	Internal	0
6	Reserved	0
7	Internal	0

Parameter flag 1

Bit	Description	
0	Internal	0
1	Data format	See "Data format" on page 21.
2 - 3	Slot diagnostics	See "Slot diagnostics" on page 21.
4 - 5	Behavior for missing modules	See "Bus controller behavior for missing modules" on page 21.
6 - 7	Reserved	0

Parameter flag 2

Bit	Description	
0 - 3	X2X cycle time	See "X2X cycle time" on page 22.
4 - 6	Async repeat	See "Slowest I/O modules" on page 22.
7	Reserved	0

3.4 Additional information for the certification authority

This section is irrelevant for the system user, but contains necessary information for certification.

3.4.1 Minimum requirements for parameter and configuration data

To set the bus controller to DATA EXCHANGE mode, at least 7 bytes of parameter data and 5 bytes of configuration data must be sent to the bus controller.

Parameters: 0x80 00 00 0B **BC 20** 00
Configuration: 0xC2 03 03 0F A0

The bytes **BC 20** in the parameter data must be replaced with the PROFIBUS DP ID of the corresponding device.

The configuration data provided is delivered by the bus controller if the configuration is read with the GetConfig service directly after switching on the device.

3.4.2 Parameter data for the operation of other I/O modules

To operate modules other than the one described above, the parameter frame must be set up as follows:

7 bytes PROFIBUS standard parameters + 6 bytes device-specific parameters + parameter bytes for the modules being used (see GSD file).

3.4.3 Checking the parameter and configuration data

The bus controller checks the received parameter and configuration data for length and plausibility.

Parameter data with a length of at least 7 bytes is generally considered valid, and a PrmFault is not output.

Both frames are checked and a CfgFault is output if an error is detected only after the corresponding configuration data has also been received.

4 Diagnostics

4.1 LED status indicators

4.1.1 State diagnostics via the Status/Error LEDs

The condition of the PROFIBUS DP bus controller is diagnosed using the LED status indicators "STATUS" and "ERROR".

STATUS (green)	ERROR (red)	Function	Solution
Off	Off	HARDWARE FAULT / POWER FAILURE	• Check wiring of supply voltage.
On	On	BUS OFF • Baud rate not detected • No connection to the DP master • DP master not active	• Check the PROFIBUS network • Check the PROFIBUS master
On	Blinking	WAIT FOR CONFIG • Transfer rate has been detected, but the PROFIBUS master has not yet configured the bus controller	• Check the node number switch • Check the slave address in the master configuration
Blinking	Off	DATA EXCHANGE - DIAGNOSTICS • The bus controller is still initializing the I/O modules • The I/O modules configured by the master cannot be found • An error has occurred on one or more I/O modules (short circuit, etc.)	• Initialization can take a few seconds depending on the number of I/O modules connected • Check the wiring and power supply for the I/O modules • Read diagnostic messages in the respective PROFIBUS master's engineering tool
On	Off	DATA EXCHANGE • Cyclic data exchange with the PROFIBUS DP master	
Blinking	Blinking	CONFIG ERROR • One or more I/O modules found do not match with the configuration of the PROFIBUS DP master • The configuration received from the PROFIBUS master is invalid	• Check the wiring of the X2X Link and the order of I/O modules • Check configuration of the PROFIBUS master • Read diagnostic messages in the respective PROFIBUS master's engineering tool • Check the configuration being used - it is possible that the number of configured I/O modules is too high
Off	Blinking	SERVICE MODE - BOOT • The bus controller's node number has been set to 255 (0xFF) - after 2 s the bus controller starts in service mode	• Set a valid node number
Single flash	Single flash	HARDWARE FAULT	

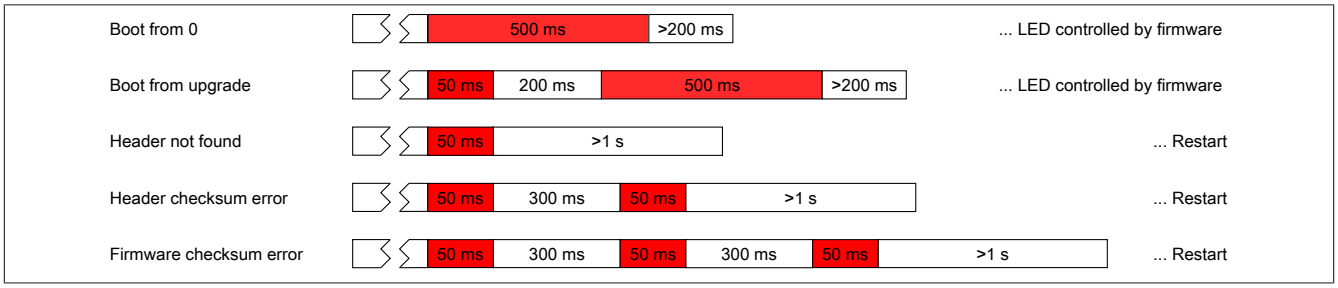
4.1.2 Communications LEDs

Some modules (for example the X20BC0063) have two orange communication LEDs in addition to the STATUS/ERROR LEDs:

- RXD PROFIBUS - Activity on the PROFIBUS network
- TXD PROFIBUS - The bus controller is transmitting PROFIBUS telegrams to the master.

4.1.3 LED blink code when switched on

The boot loader indicates the following states on the "MS" module status LED:



If faulty firmware in the flash memory causes an error during booting, then the system will attempt to reboot using the factory default boot block.

This means that if an error occurs in the firmware upgrade sector, the module will automatically revert to the factory default sector (boot from 0).

4.1.4 Forcing a boot from the factory default sector

This is necessary if firmware has been stored in the upgrade sector, operates the watchdog correctly but doesn't allow the booting process to occur without errors. The boot loader simply starts the defective firmware and doesn't provide a way to carry out a subsequent update.

To force a boot from the factory default sector, one of the network address switches must be continuously moved during the actual boot procedure. This is detected by the bootloader, which causes the "MS" module status LED to begin flashing red quite very rapidly. After 1 second passes where the network address switch is no longer changed, the bus controller restarts using the factory default boot sector and the current network address switch.

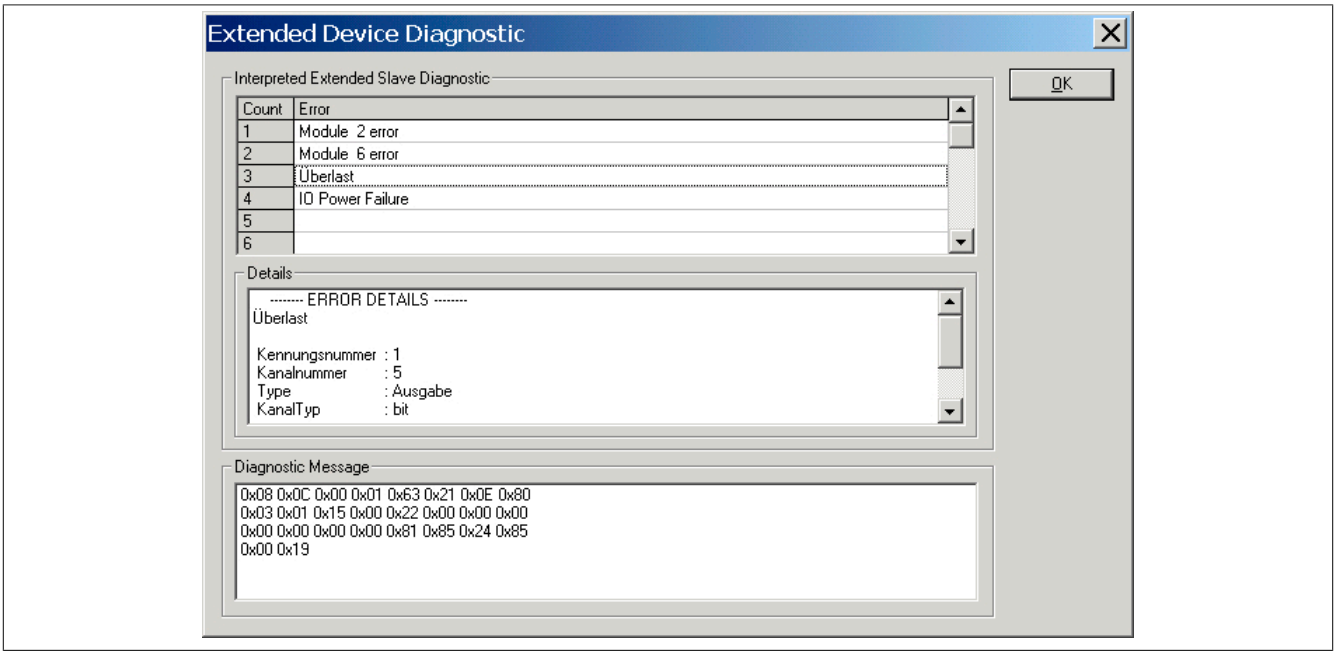
4.2 PROFIBUS DP diagnostics telegram

When an error message occurs, a diagnostics telegram is sent from the bus controller to the PROFIBUS DP master. The data within is evaluated and displayed in different forms depending on the engineering tool.

4.2.1 Displaying diagnostics information in the engineering tool

How diagnostic data is displayed depends on the engineering tool being used.

Normally, messages from the diagnostics telegram are displayed as plain text:



4.2.2 Evaluating the diagnostics telegram during runtime

With most DP master systems, it's possible to evaluate the information delivered with the diagnostics telegram using software.

B&R master

Evaluation with the DPMSlaveStat() and DPMSlaveExtStat() functions from the DPMaster library.

Siemens master

Evaluation with SFC13

Other master systems

The required information must be obtained from the manufacturer of the respective master system.

4.2.3 Boot behavior

Improved boot behavior starting with firmware version 1.32:

After the master has configured the slave (with SetParameter and CheckConfig), it provides static diagnostics after a few seconds have passed. During this time, there is a delay until the connected I/O modules have been started and configured. Then static diagnostics is taken away and all I/O modules are activated simultaneously.

4.2.4 Structure of the diagnostics telegram

The bus controller sends a diagnostics telegram with a length of 20 to 56 bytes. The contents correspond to the PROFIBUS DP standard "PROFIBUS DP standard DIN19245-3".

The length of the telegram depends on the type and number of error messages:

Byte	Description		
0	See "PROFIBUS DP standard DIN 19245-3"		
1	See "PROFIBUS DP standard DIN 19245-3"		
2	See "PROFIBUS DP standard DIN 19245-3" (bit 7 = Diag.Ext_Diag_Overflow)		
3	Address of the master		
4	Bits 8 through 15 of the Device ID		
5	Bits 0 through 7 of the Device ID		
6	Header byte for device-specific diagnostics (always 0x0E)		
7	Diagnostic flag 1 (see "Diagnostic flag 1" on page 28)		
8	Diagnostic flag 2 (see "Diagnostic flag 2" on page 28)		
9	Whole number portion of the version number for the bus controller		
10	Decimal portion of the version number of the bus controller (**Example** Byte 9 = 0x01, Byte 10 = 0x0C → Firmware version = 1.12)		
11	Internal error (see "Internal error" on page 29)		
12 - 19	I/O module error, 64-bit. Each bit identifies the state of one I/O module (0 = no error, 1 = error)		
"Slot diagnostics = S7 format" (see "Configuration" on page 19)		"Slot diagnostics = Default" (see "Configuration" on page 19)	
20	Header byte for slot diagnostics (always 0x49)	20 - 22	Single channel error[1)]
21 - 28	Copies of bytes 12 through 19	23 - 25	Single channel error[1)]
		26 - 29	Single channel error[1)]
29 - 31	Single channel error[1)]	29 - 31	Single channel error[1)]
32 - 34	Single channel error[1)]	32 - 34	Single channel error[1)]
...	...	...	...

1 See section "Single channel error" on page 29.

4.2.4.1 Diagnostic flag 1

Bit	Description
0	E100: Insufficient resources on the bus controller Check the module arrangement with the B&R BC PROFIBUS Design Tool
1	E101: Too many I/O modules configured • Increase the cycle time • Check the module arrangement with the B&R BC PROFIBUS Design Tool
2	E102: Configuration error • The I/O modules actually connected do not match with the master's configuration • Check the order of the I/O modules on the X2X Link network Check the order of the I/O modules in the master configuration
3	E103: Version conflict between the GSD file and the firmware • Adjust the engineering tool to an older version of the GSD file if it still meets the requirements for the application Update the firmware on the bus controller
4	E104: I/O modules can no longer be configured after the service channel
5	E105: Too much cyclic data was configured • Increase the X2X Link cycle time (see "X2X cycle time" on page 22)
6	E106: X2X Link network warning • Problems with the X2X Link wiring One or more I/O modules on the X2X Link network are too slow for the configured I/O cycle (see)
7	Set to 1 if the master should evaluate the device-specific diagnostics. (various engineering tools do not evaluate the other bits if this bit is 0)

4.2.4.2 Diagnostic flag 2

Bit	Description
0 - 3	Status of the bus controller (see "LED status indicators" on page 25) 1) BUS OFF 2) WAIT FOR CONFIG 3) DATA EXCHANGE - DIAGNOSTICS 4) DATA EXCHANGE 5) CONFIG ERROR
4	E112: Internal error • An internal error has occurred. Evaluate the value in Byte 11 of the diagnostics telegram
5 - 7	Reserved

4.2.4.3 Internal error

This error can occur if a GSD has been improperly manipulated. If this error occurs with an unmodified GSD file, please contact B&R Support.

4.2.4.4 Single channel error

If a single channel error is not present, then the bytes intended for it are not transferred. A 3-byte array containing the error description is transferred for each error queued.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 0	1	0	I/O module number (0 to 63)					
Byte 1	Output	Input	Channel number (0 for module-referencing errors, 1 to 63 for single channel errors)					
Byte 2	Channel type (1=1 bit / 5=16 bits)			Error number				

The maximum number of single channel errors that are reported at a time depends on the type of bus controller:

Bus controller	X67BC6321	X67BC6321.L08 X67BC6321.L12 X20BC0063
Maximum number of single channel errors during slot diagnostics = Default / S7 format	12 / 9	14 / 11
Maximum size of diagnostic frame	56 bytes	62 bytes

If more errors are present at one time than can be reported in the diagnostics frame, Byte 2 / Bit 7 (Diag.Ext_Diag_Overflow, see "Structure of the diagnostics telegram" on page 28) in the diagnostics telegram is set to indicate to the master that there are still errors queued. The master can only receive the additional error messages if the current errors have been corrected.

Error numbers 1 through 15 are defined in the PROFIBUS DP standard. The bus controller uses the following numbers:

4	Overload
5	Overtemperature
6	Open line
7	Upper limit value exceeded
8	Lower limit value exceeded
9	Error (depending on the diagnostics options on the particular I/O module)

Error numbers 16 through 31 are vendor-specific and entered in the GSD file:

16	Firmware not installed on the I/O module
17	Power supply warning 1
18	Power supply error 1
19	Power supply warning 2
20	Power supply error 2
25	I/O supply missing or X20 module not installed
26	Overload group 1
27	Overload group 2
28	Overload

5 Use with SIMATIC Manager

Requirements

Software

The SIMATIC STEP7 V5.4 software package from SIEMENS is used as the engineering tool. All following screenshots were taken with this version. B&R PROFIBUS DP bus controllers can also be easily integrated into other software versions, however. The appearance of the user interface can vary. There should not be any difficulties integrating the bus controllers if this document is used as a reference.

Hardware

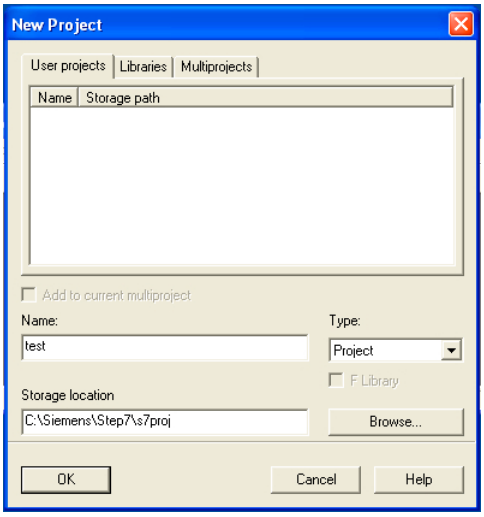
A PROFIBUS master is required for using any of the B&R PROFIBUS DP bus controllers. A SIMATIC S7-300 station with the CPU315-2DP was selected as the example configuration. It takes on the function of the PROFIBUS master and serves as the starting point for integration. An online connection is required In order to program the CPU and access it for diagnostics. For options to configure the programming interface, e.g. using a PC adapter, see the SIMATIC Manager help documentation as well as the corresponding user documentation.

5.1 Project environment

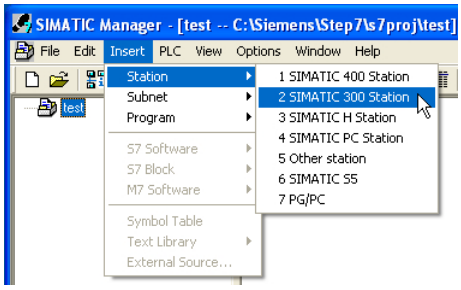
A new GSD file can only be added to an open project. An existing project can be opened or a new one created. This can be done by using wizard "New project" or via manual input.

5.1.1 Creating a new project manually

● A new project can be created in the SIMATIC manager using the menu bar below: *File → New*. Under tab "User projects", you can assign a project name (in this case "test") and choose where to save the project. Select "Project" as the project type. Settings in the two tabs "Libraries" and "Multiprojects" are not necessary.

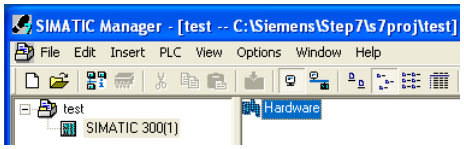


● When the project is created, the hardware must be configured. Under menu option *Insert → SIMATIC 300*, a SIMATIC 300 station can be added. The user can choose a name for the station. Proposed name "SIMATIC 300(1)" was used here.

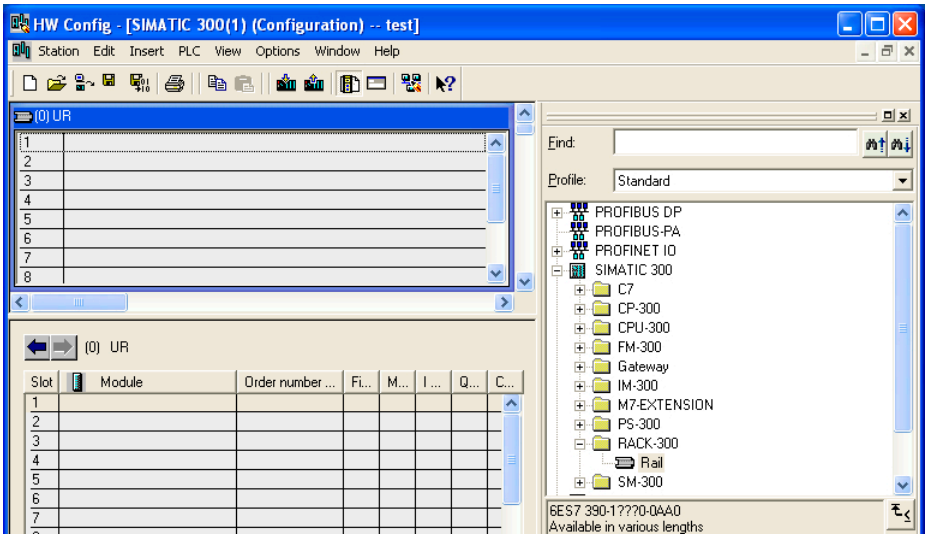


The selected SIMATIC 300 station is then listed in project folder "test".

● When selecting the SIMATIC 300(1) station, an icon appears in the right window for configuring the hardware. A double-click opens the hardware configuration window.



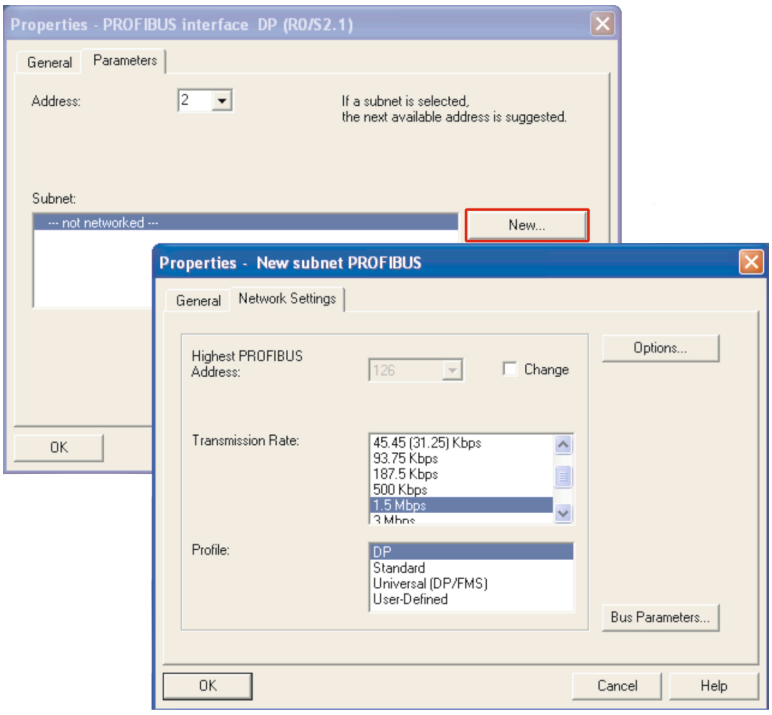
In order to add the desired components, the Hardware Catalog must be made visible under menu option *View → catalog*. Alternatively, components can be added via menu option *Insert → Insert object*.



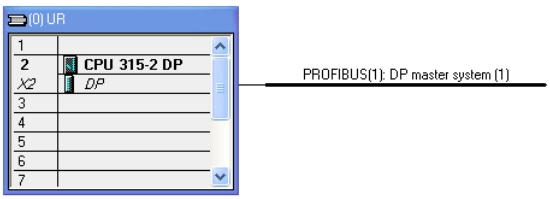
A top-hat rail is used as the foundation for further configuration (SIMATIC300/Rack300/Rail). The CPU315-2DP is then added to this (SIMATIC300/CPU-300/CPU315-2DP). This is only possible on slot 2, since slot 1 is reserved for the power supply.

After it is added, a configuration window is opened for the fieldbus connection. If the project does not yet have a PROFIBUS connection, a new one can be created using button "New". The engineering tool automatically suggests a name (PROFIBUS(1)) as well as the subnet ID. The subnet ID is a combination of the project number and the subnet number. This is important if you want to go online with a programming device and no corresponding project exists.

If no other entries are known, the values suggested by the engineering tool can be used. Making settings under tab "Network settings" is not necessary. The automatically entered values correspond to a standard PROFIBUS configuration. This also applies to settings "Options" and "Bus parameters". The baud rate can be set between 9.6 and 12000 kbit/s. The X20BC0063 and X67BC6321 are both equipped with automatic baud rate detection and support all available baud rates.

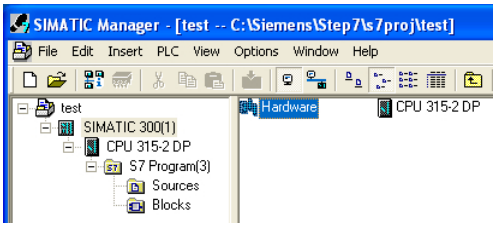


The following figure shows the CPU315-2DP on slot 2 and the established network connection PROFIBUS(1).

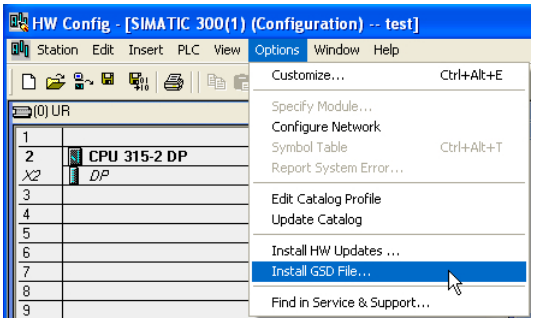


5.2 Installing the GSD file

The GSD file can only be imported using the hardware configuration user interface. This can be opened by clicking once on station "SIMATIC 300(1)" and then double-clicking on "Hardware".



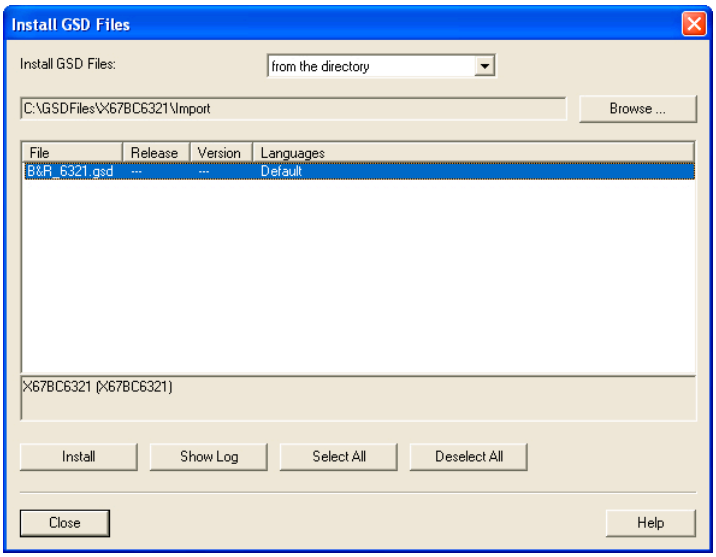
Select function "Install GSD file" in menu option "Options".



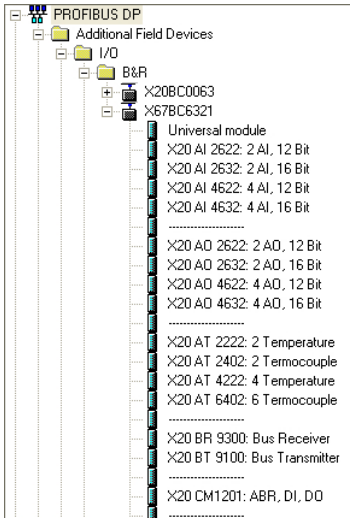
In the window that opens, you can choose to install the GSD file from a Step 7 project or from another directory. Function "Browse" specifies the associated path. The GSD files to be added are listed in the lower area of the window.

GSD files can be added to the Hardware Catalog with button "Install". Note that integrating new GSD files cannot be undone. A successful installation is confirmed via a message box.

Selection window for GSD files being imported:

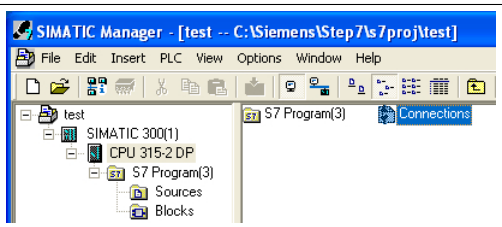


After selecting and installing the GSD file, the imported B&R PROFIBUS DP bus controllers are found in folder PROFIBUS DP / Additional field devices / I/O / B&R. They are now completely integrated and can be configured with all corresponding I/O modules.



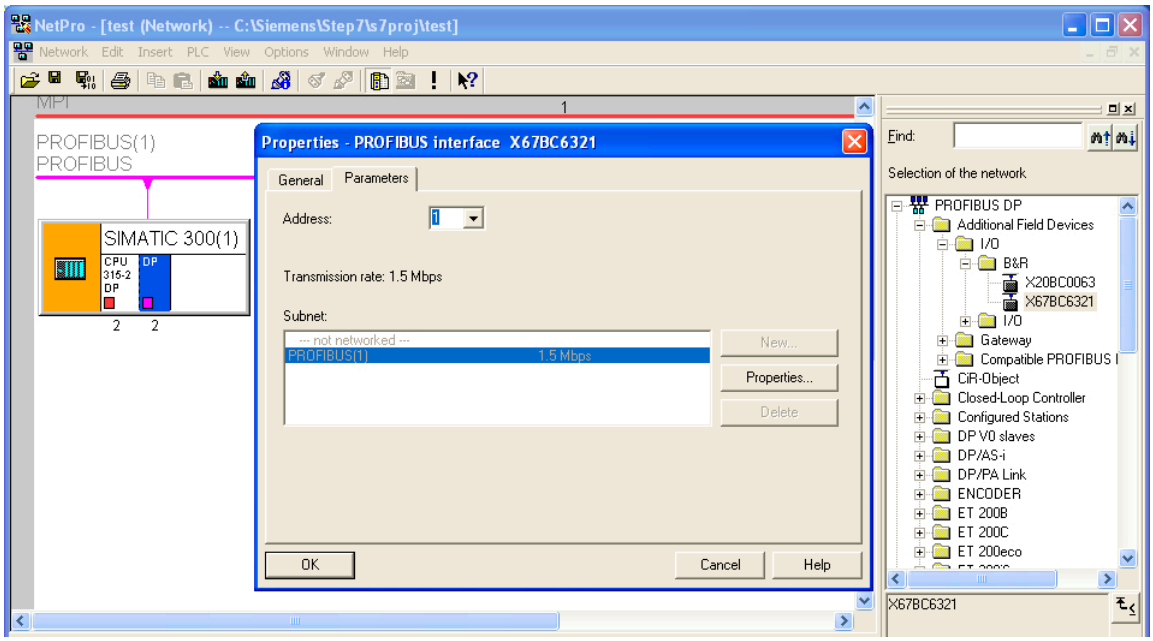
5.3 Integrating PROFIBUS DP bus controllers

B&R PROFIBUS DP bus controllers are added in network connection view "Connections". This can be opened when CPU315-2DP is selected.



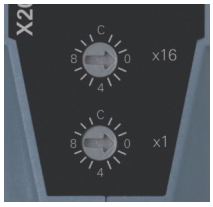
For a successful connection of the PROFIBUS DP bus controller, it is necessary that the DP interface of the SIMATIC 300(1) station is active on the CPU315-2DP. This can be recognized by colored highlighting (see figure).

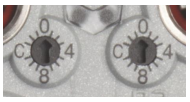
After integrating the bus controller, a configuration window opens. The only thing to configure is the address. All other settings can be left as they are. The selected addresses must match the node number set on the bus controller!



Information:

Both X67 and X20 PROFIBUS DP bus controllers only take on the newly assigned node numbers after a restart!

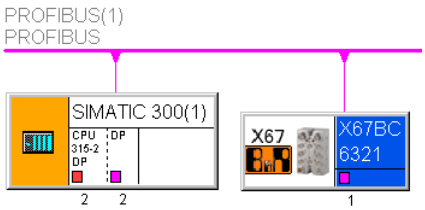




High Low

On the X67BC6321, the left must be multiplied by 16.

After a successful integration, the configuration should look like this:



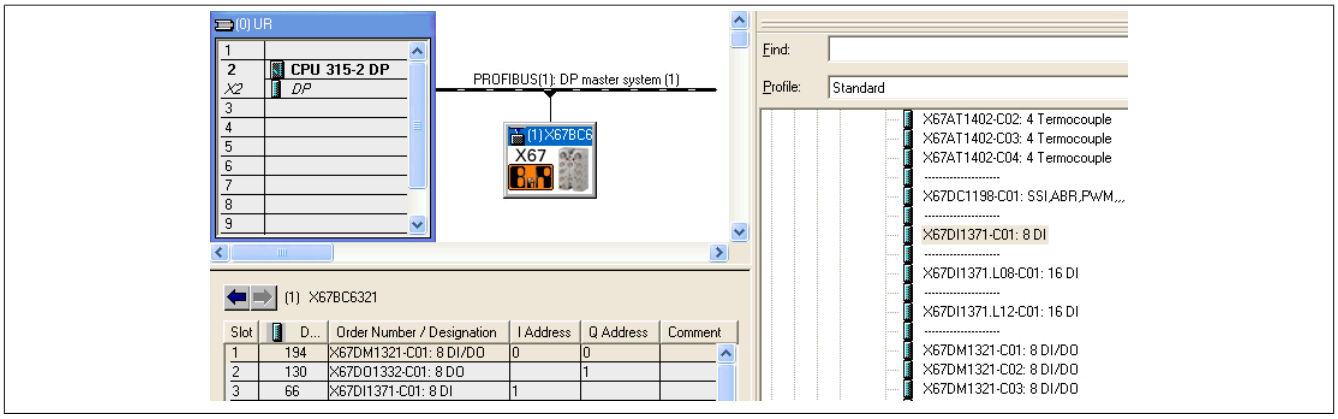
5.4 Extending X2X Link

Open the corresponding hardware configuration by double-clicking on the B&R bus controller symbol in the network view. The desired I/O modules can be added to the bus controller from the Hardware Catalog.

In contrast to the procedure for the B&R BC Design Tool, the sequence in which the modules are added plays a key role here. The positions / slot numbers of the I/O modules must match the actual physical structure.

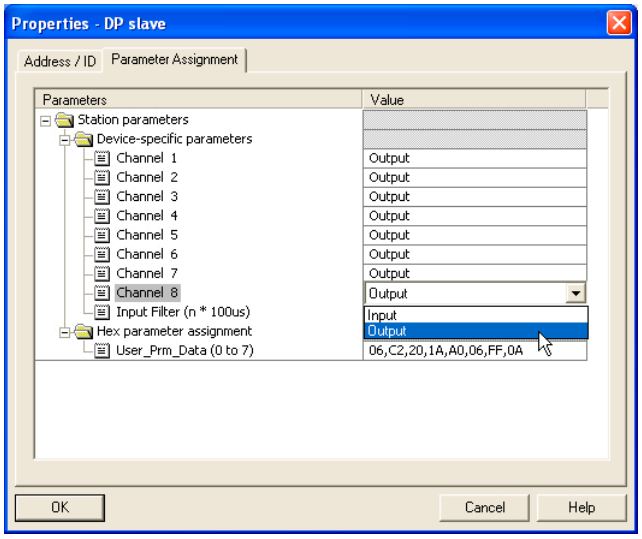
Since PROFIBUS DP bus controller X67BC6321 includes module X67DM1321, this is automatically positioned at slot 1. For configurations with X20 bus controller X20BC0063, the required X20PS9400 power supply module is in the first slot position. All other slot assignments can be chosen freely.

In the example, an X67DO1332-C01 and an X67DI1371-C01 are connected to the X2X Link. The engineering tool assigns the I/O addresses and does not require any further attention for the time being.



5.4.1 Configuring the I/O modules

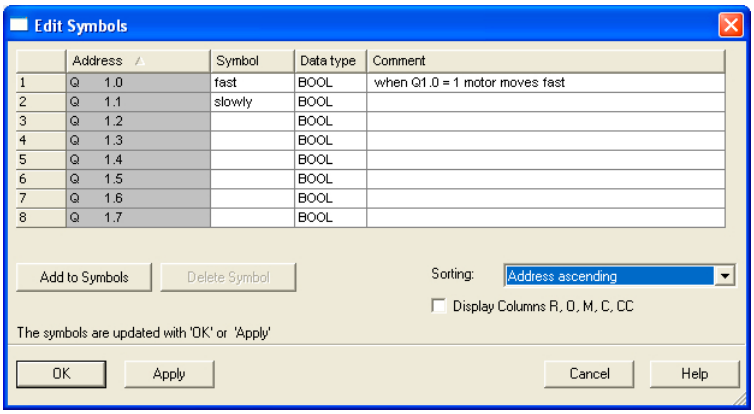
The various I/O modules can be configured by right-clicking and selecting "Object properties".



Addresses can be assigned manually under tab "Address/ID". In folder "Device-specific-parameters" in section "Parameter assignment", it is possible to manually assign the digital channels of the X67DM1321 their function as inputs or outputs, for example. Default values under the name "Hex parameter assignment" should not be modified. These hex number combinations are automatically generated from the selected configuration. If a particular I/O module does not require configuration, then folder "Device-specific parameters" is not displayed.

5.4.2 Variable assignment

Variable names can be assigned in window "Edit symbols". Right-clicking on an I/O module opens the configuration window for that module. Each channel can be assigned symbolic names and detailed comments.



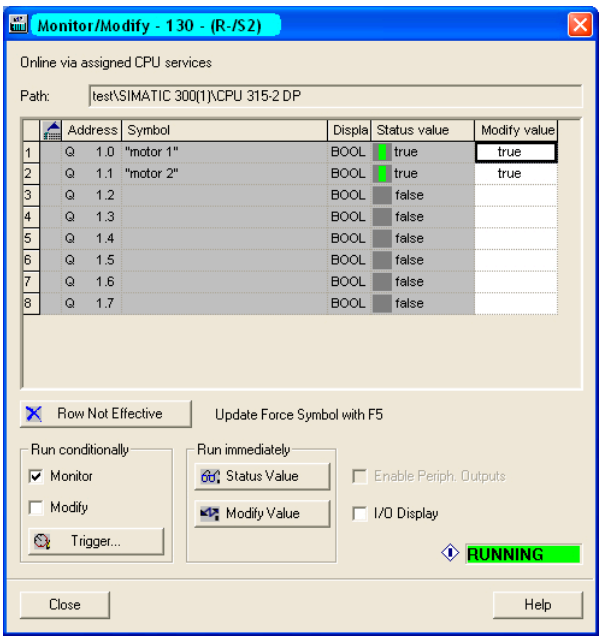
5.5 Configuration download

After stetting the desired configuration and module assignments as well as the corresponding software configuration, the configuration is transferred to the controller (CPU315-2DP). To begin the transfer process, the project must be saved and compiled. In the hardware and network views, this can be done using menu option *Station/Network →Save and compile*. The control data can be downloaded using the Download button, or with menu option *PLC→download* (download to current project) if the SIMATIC station is selected. It is also possible to download a project in the hardware or network views. After selecting which controller the new project should be transferred to, the corresponding interface can be configured. All accessible stations can be displayed via "View".

In order to program the controller, it must be temporarily set to mode "STOP". This message must then be confirmed with "OK". After the download is complete, the CPU will restart after a query.

5.6 Controlling the modules

Function "Monitor/Modify" can be used to quickly and easily test a module's outputs, for example. This can be accessed in the hardware view by right-clicking on the corresponding module. The modified values can be entered and then assigned by selecting "Modify". With function "Monitor", the inputs and outputs can be monitored and their current states displayed.



In this screenshot, outputs Q1.0 and Q1.1 of output module X67DO1332 were set to TRUE and displayed using function "Monitor". Active outputs can also be identified by the corresponding LEDs on the module.

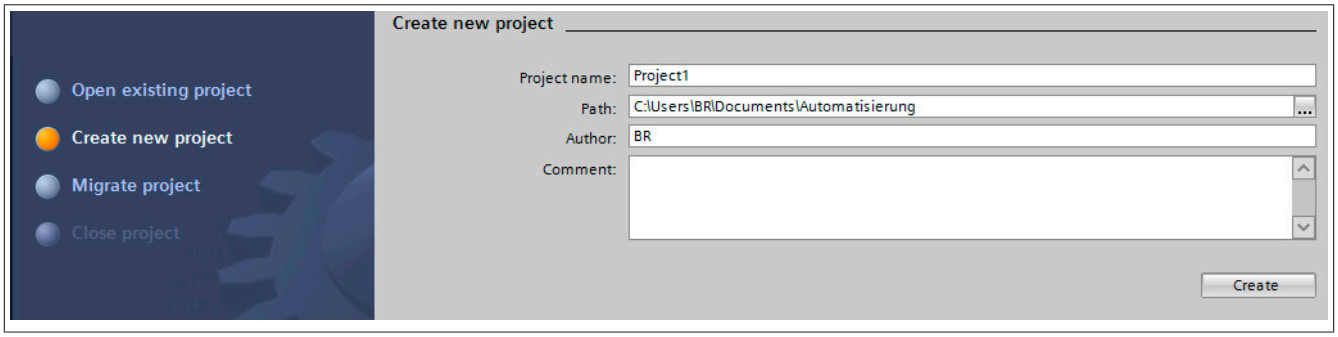
6 TIA portal

Software and hardware used for this example:

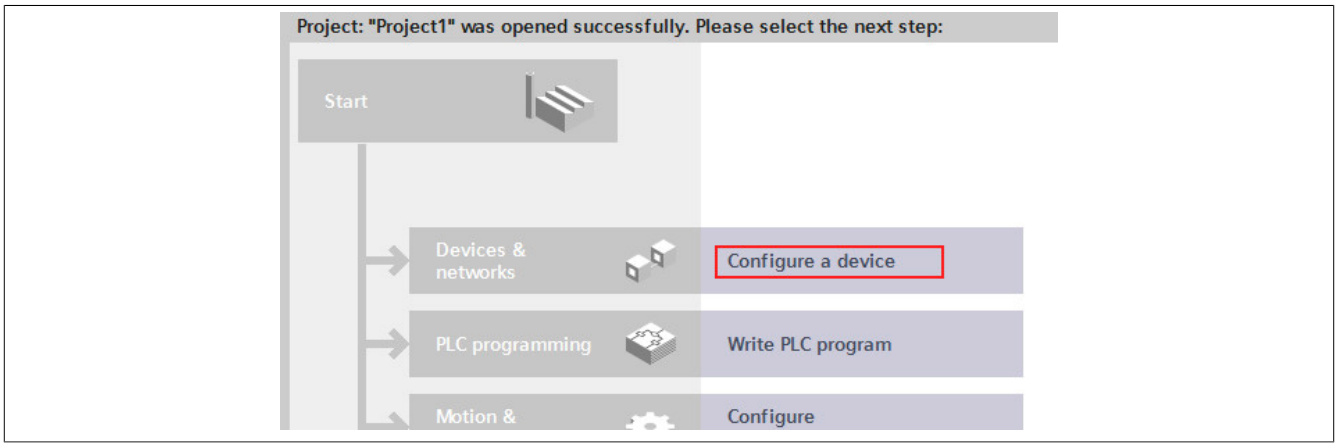
- B&R PROFIBUS bus controller X20BC0063
- GSD file from the B&R website
- CPU315-2 PN / DP Siemens CPU as PROFIBUS master
- TIA portal version 15.1

6.1 Creating a new project

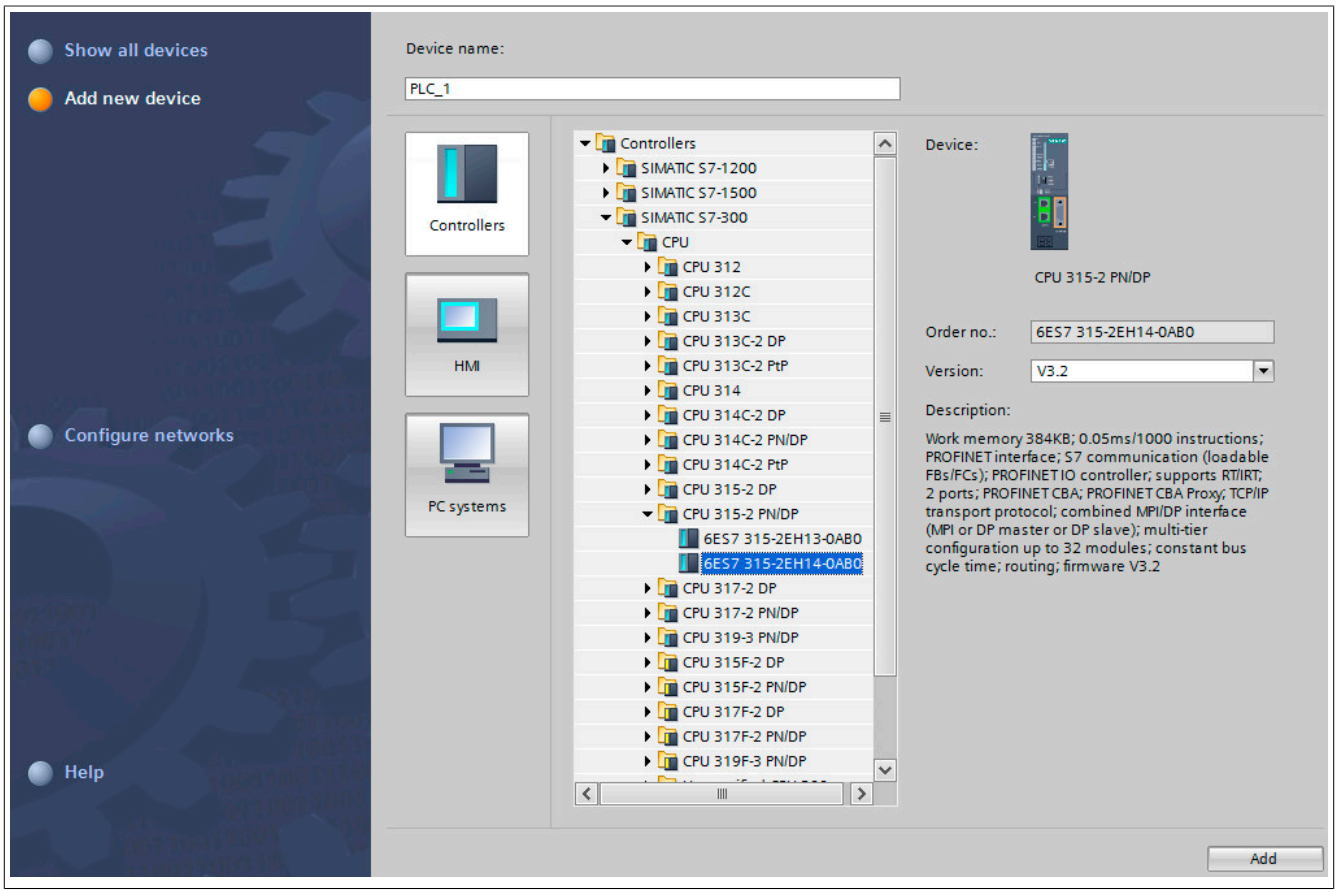
● After opening the TIA Portal development environment, a new project must first be created. To do this, select **Create new project** and specify the name and path of the new project. The new project is created with button **Create**.



● After the project is created, the necessary devices can be added and configured.
The first step is to select **Configure a device**.

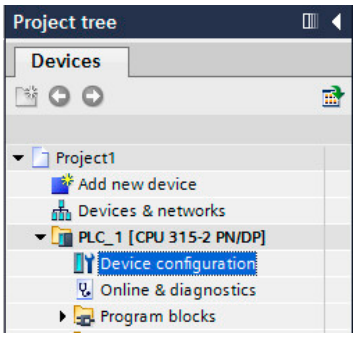


● The CPU used is selected using **Add new device** and added to the configuration with button **Add**.

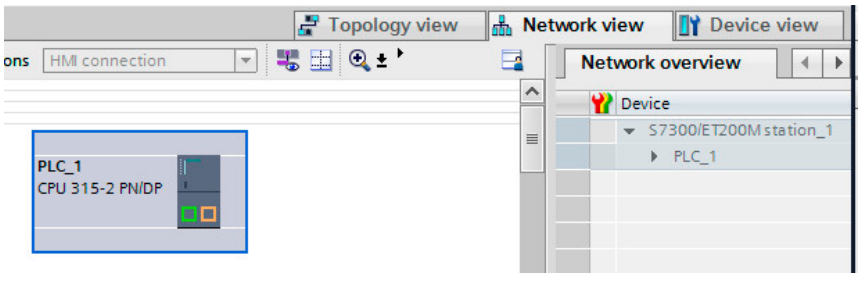


6.2 Adding a slave

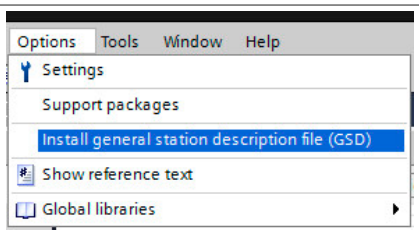
● To add a slave, you must switch to the hardware view. To do this, select **Device configuration** by double-clicking in column **Project tree**.



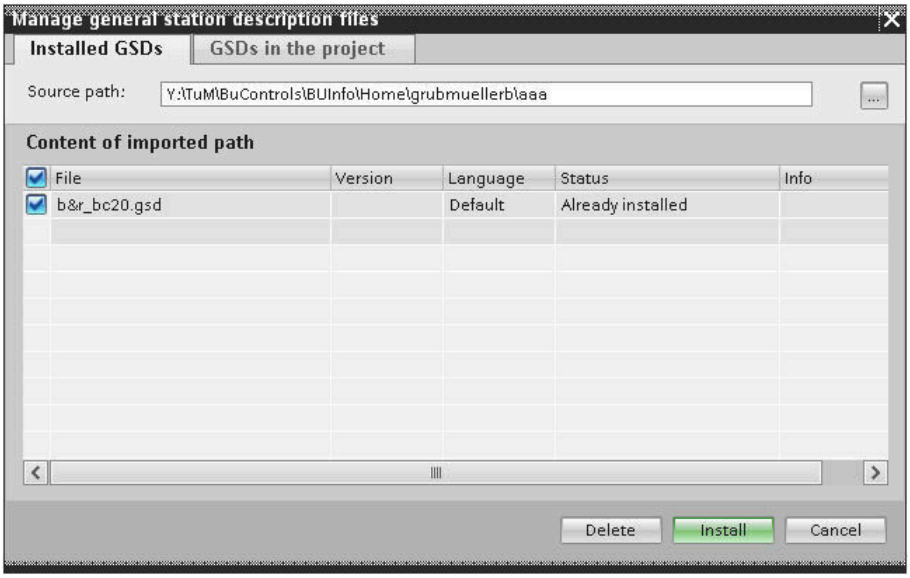
● The hardware structure can be checked or updated via tab **Network view**.



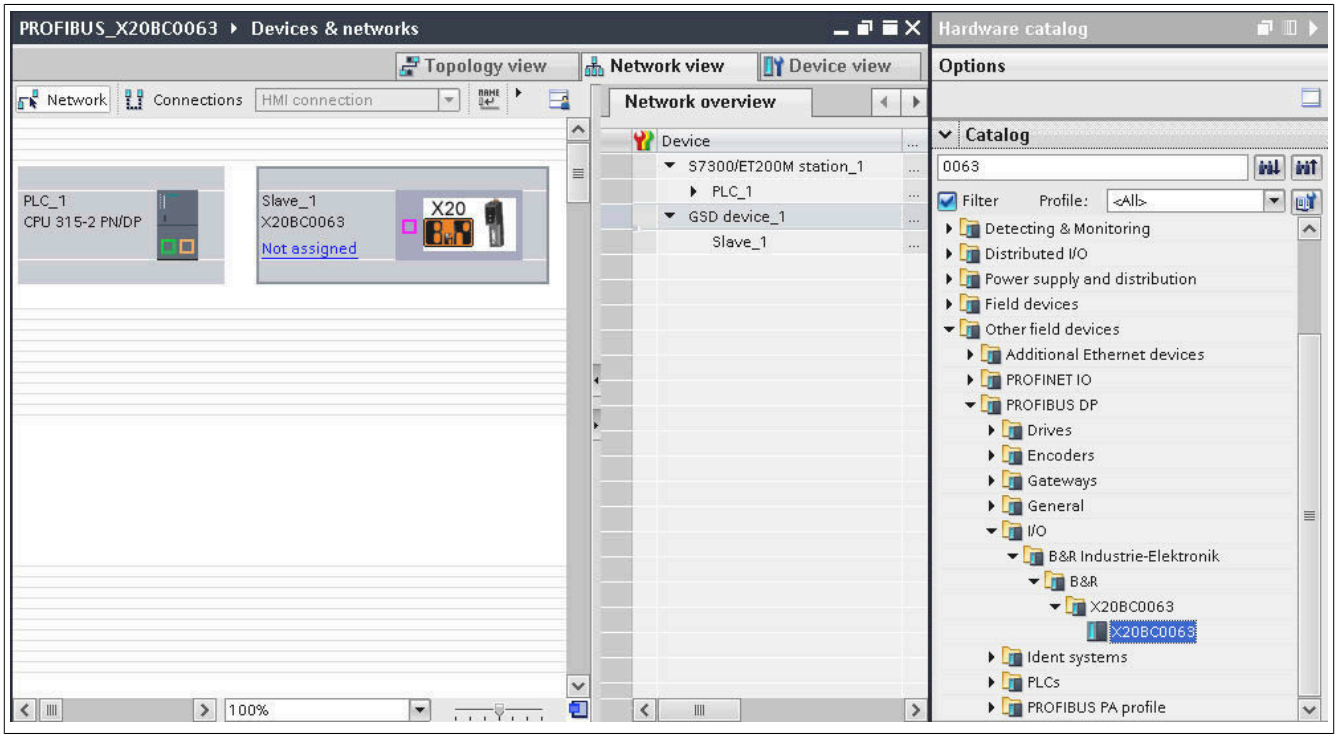
● In order to use the bus controller, its description file must first be installed. The description file can be downloaded from the B&R website and installed via *Options → Install general station description file (GSD)*.



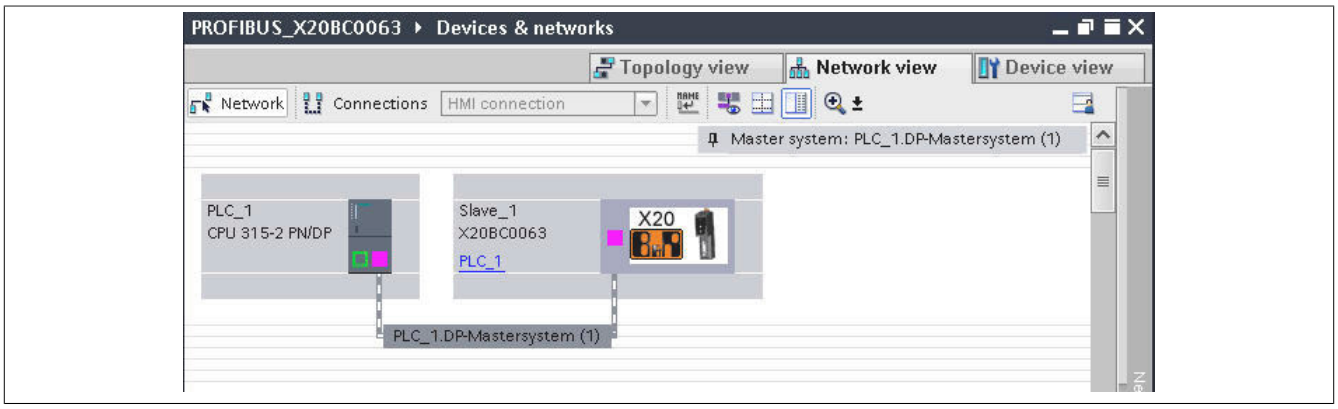
● The downloaded description file is selected in the dialog box and added to the project with button **Install**. This adds the bus controller to the Hardware Catalog of the TIA portal.



● Now the installed bus controller can be used in the project. The bus controller is selected in the Hardware Catalog and then dragged and dropped into the project.



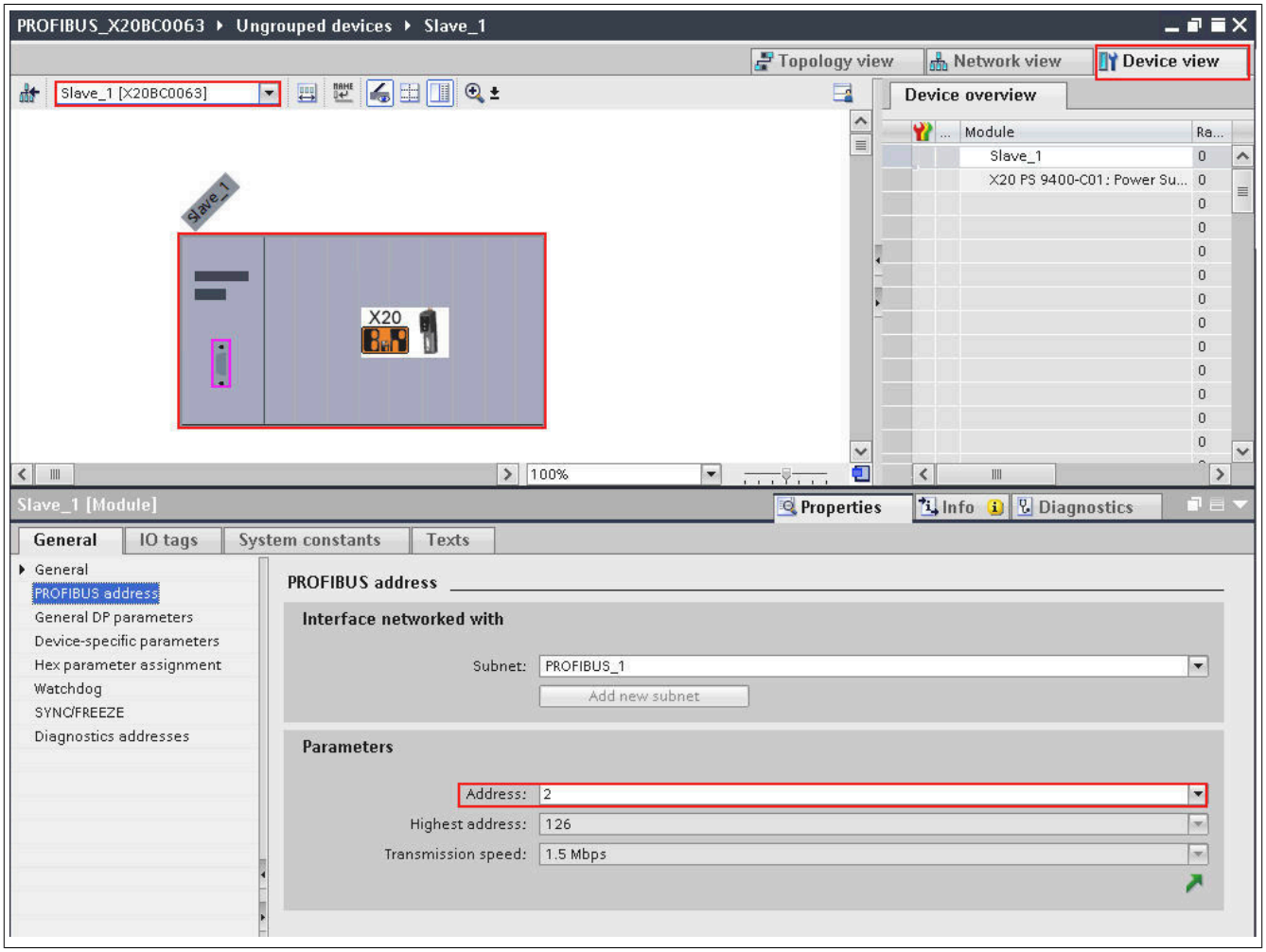
● The installed CPU and the bus controller are connected via PROFIBUS. For this purpose, the PROFIBUS interface of the CPU is connected to the PROFIBUS interface of the bus controller via drag-and-drop.



● To establish the communication between PROFIBUS master and PROFIBUS slave, the PROFIBUS address of the slave must be set.

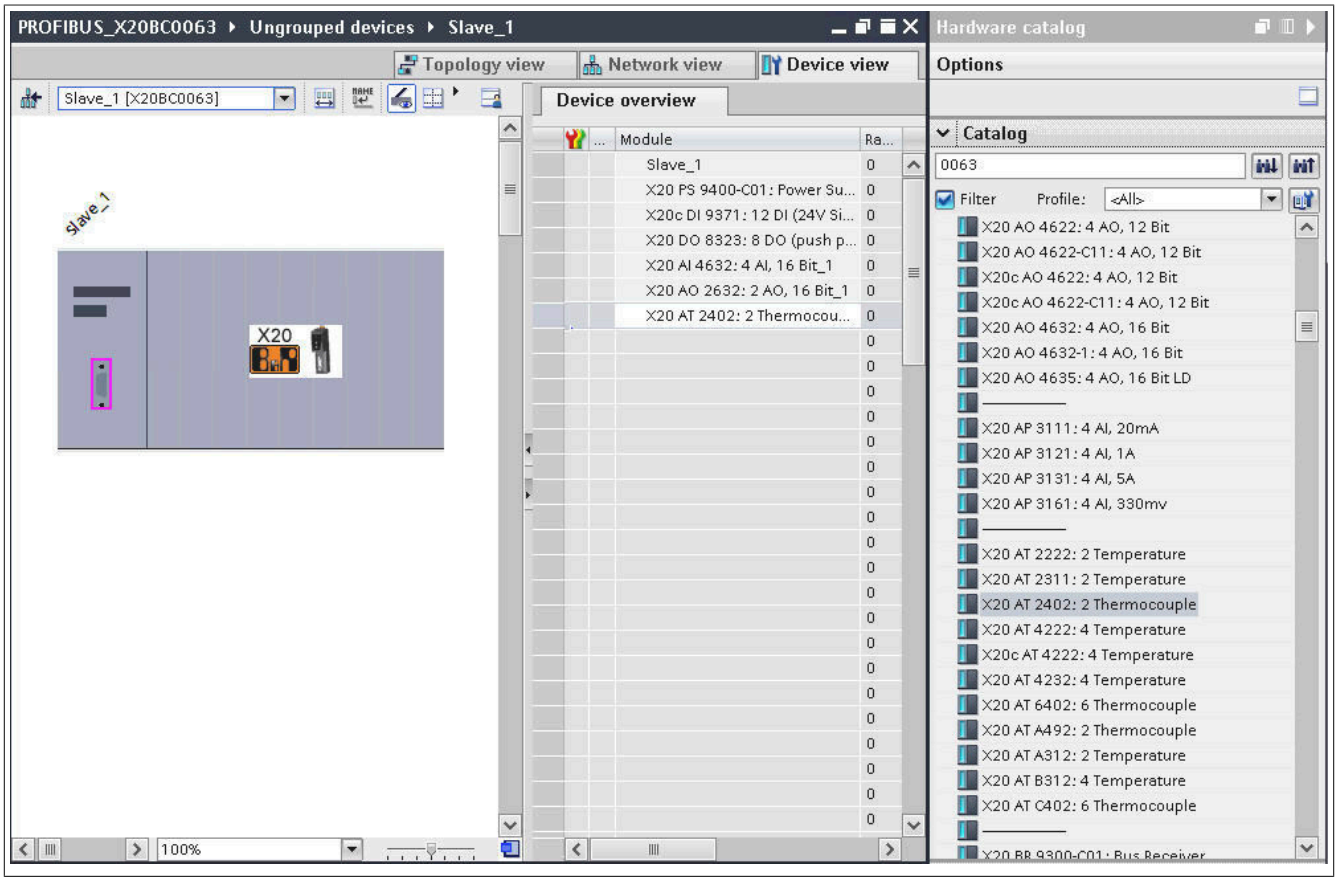
To set the PROFIBUS address in the TIA portal, select the PROFIBUS bus controller (X20BC0063) from the **Device overview** in the drop-down list.

By double-clicking on the image of the module, the setting options become visible below. The desired PROFIBUS address must be set here.



In addition, further configurations can be carried out for the module.

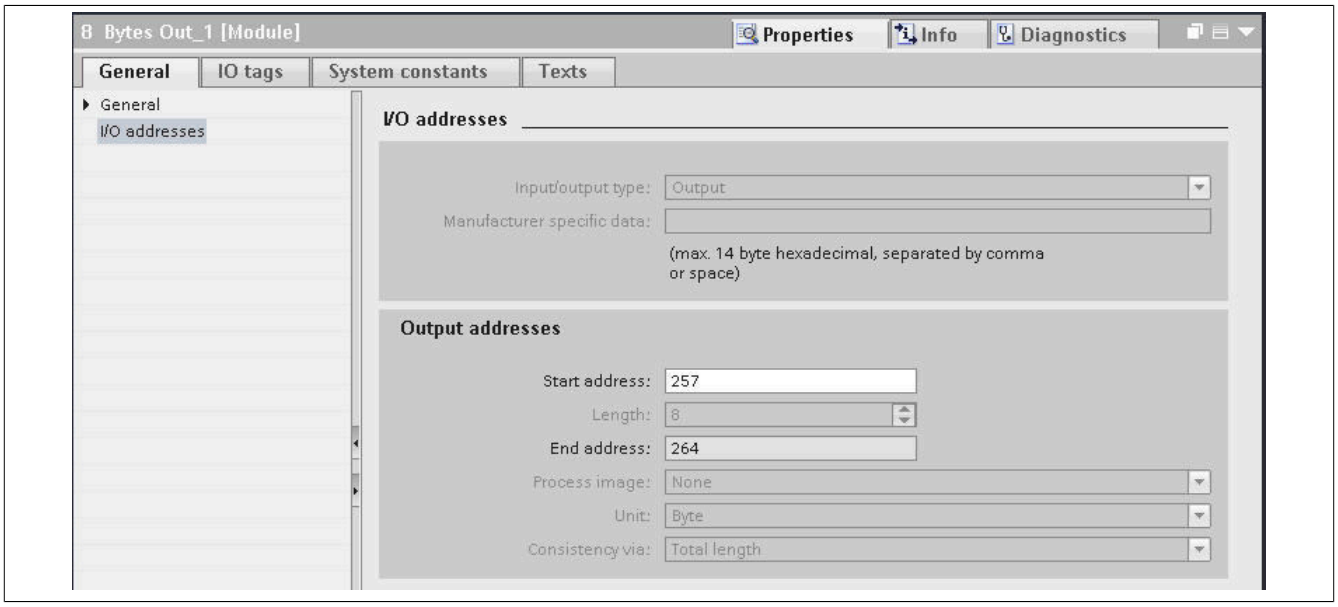
● Any additional modules can be added with the Hardware Catalog. To do this, drag and drop the modules into the **Device overview**.



● After modules are added, they can be easily configured by selecting them.

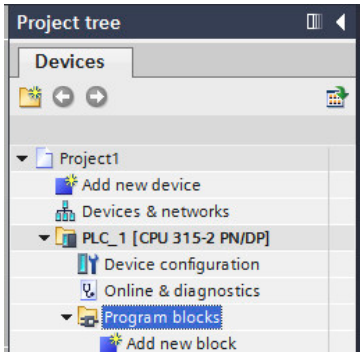
Example

"End address" of a module is read out via *Properties* → *General* → *I/O addresses* in order to be able to link it with a variable created in the application.

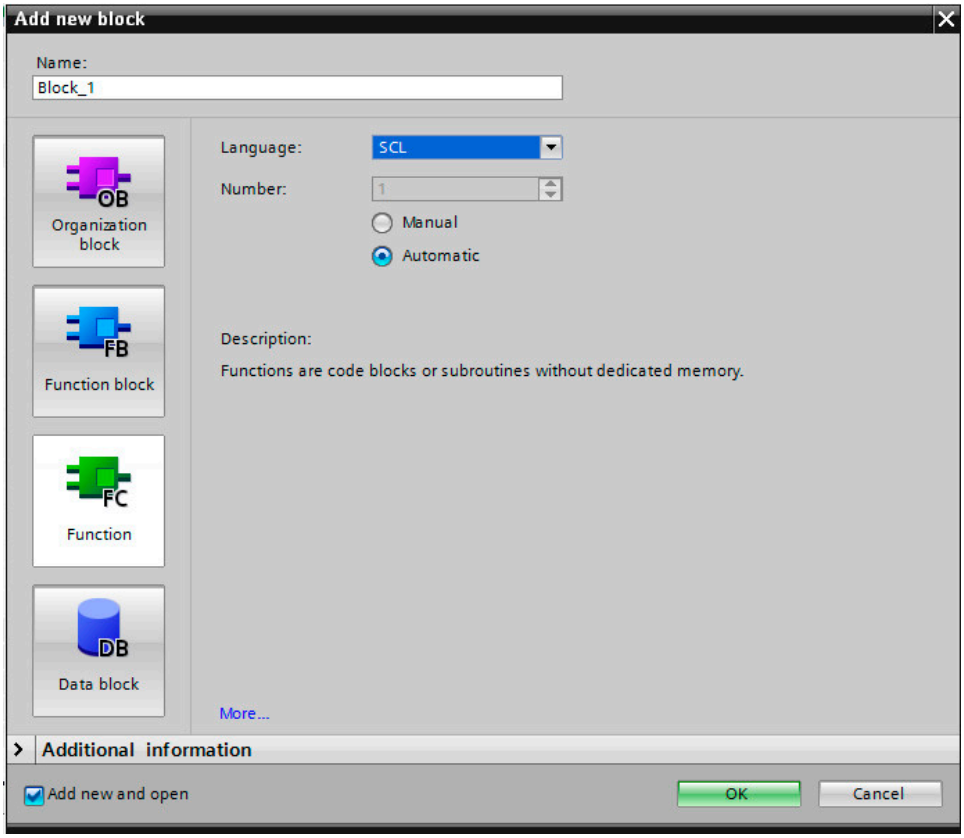


6.3 Creating an application

● An application can be added via *Project tree → Program blocks*.



● If a new program is created using **Add new block**, the name of the block and the programming language are first set and confirmed with **OK**.
In this example, this is **SCL** (Structured Text), but any programming language can be used.

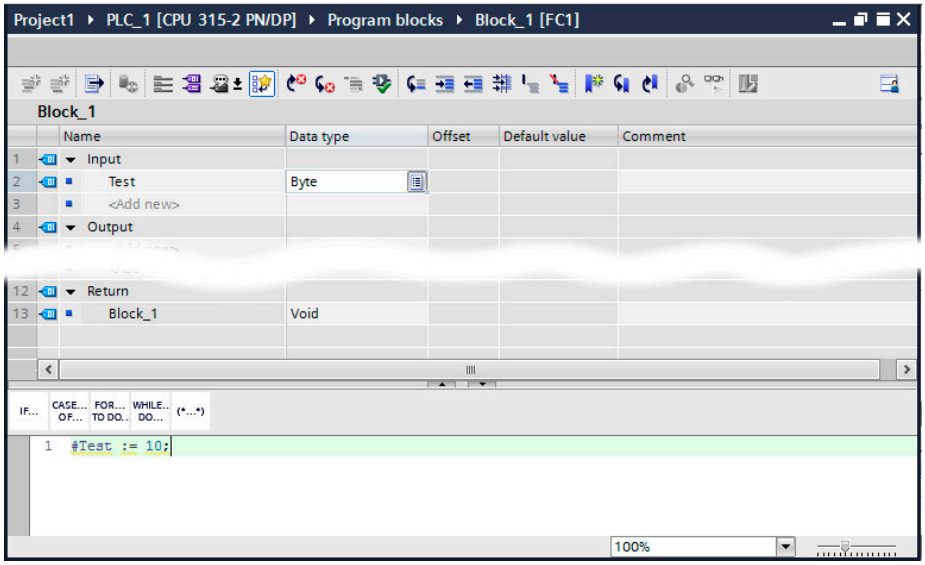


● The block is divided into two parts.

- Variables can be created in the upper part of the block.
- The application is programmed in the lower part.

Example

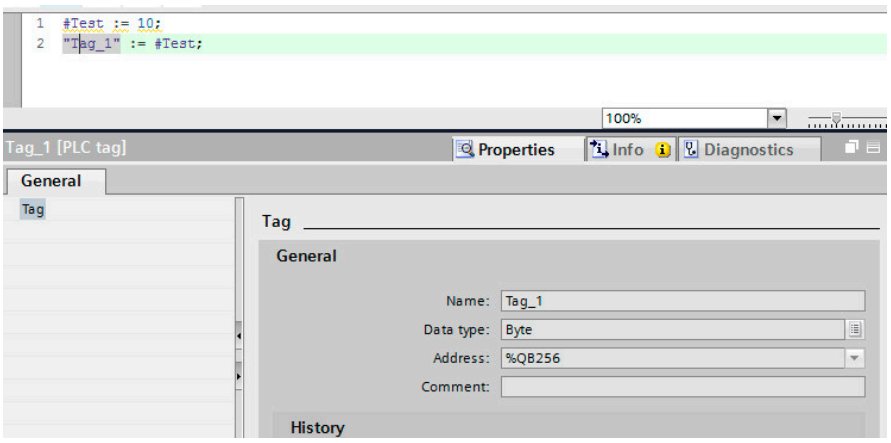
A variable named "Test" of data type "BYTE" should be created and assigned value 10 using the application.



● A **tag** can now be created in the application to link the variable to an output via an address. This is created with "%QB + Address" or "%IB + Address":

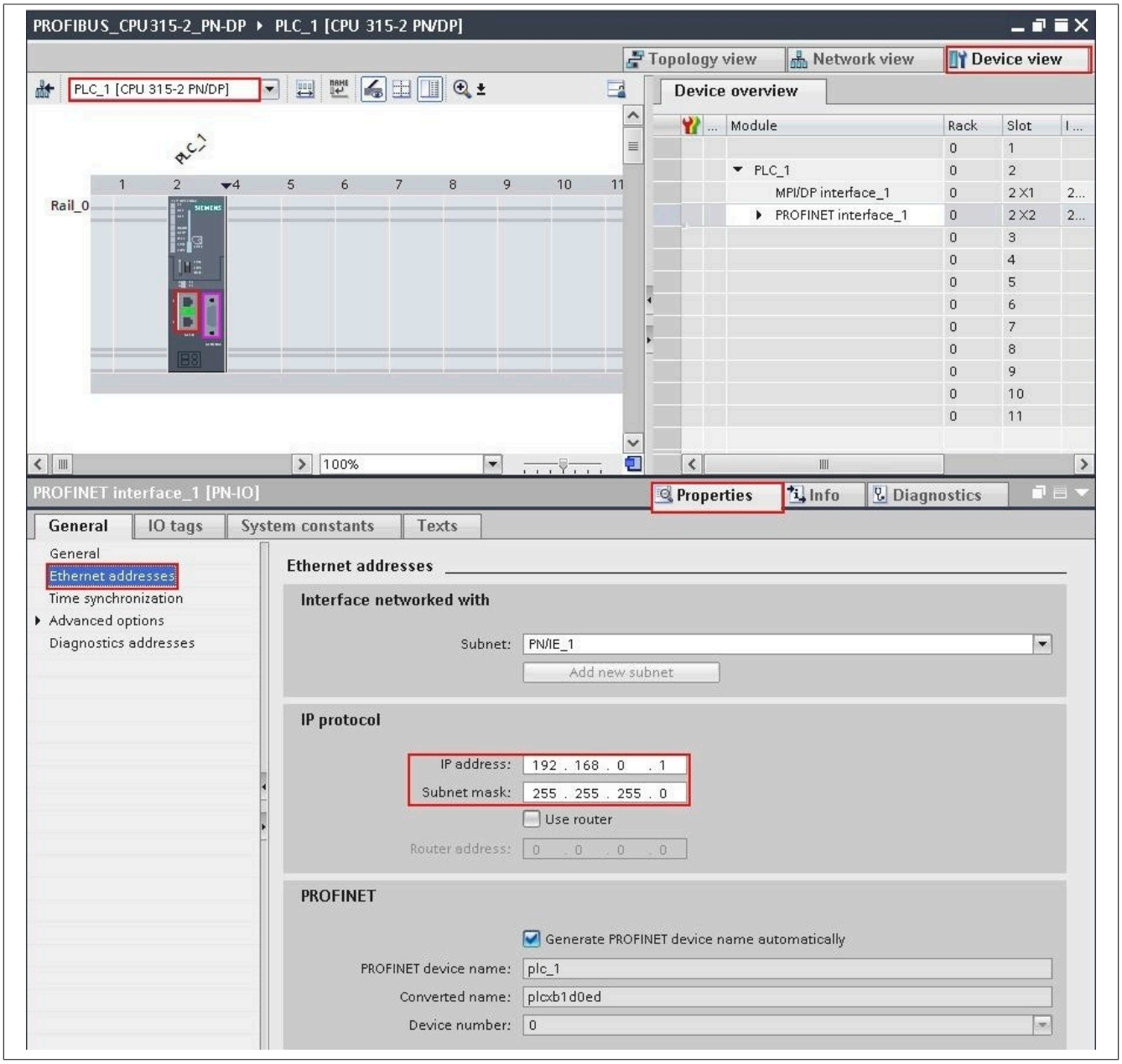
Example

Tag %QB256 is assigned to variable "#Test".

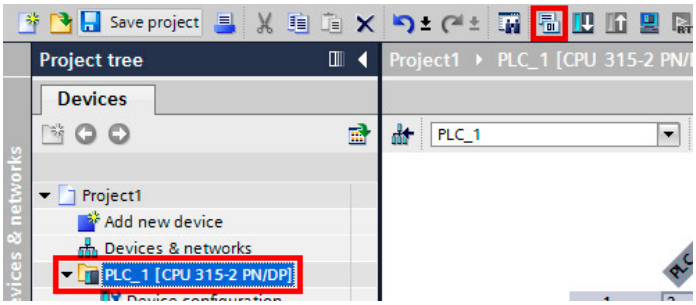


6.4 Establishing a connection to hardware

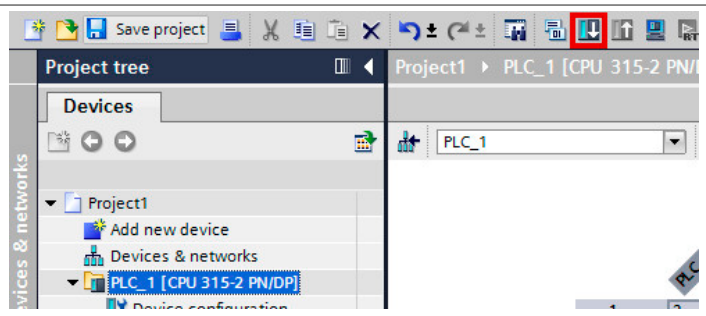
● To establish a connection from the TIA portal to the CPU, the IP address and CPU subnet mask must be configured in the TIA portal. To do this, select the CPU in the **Device view**. Clicking on the Ethernet interfaces with the mouse opens the corresponding window in menu "Properties". The IP address and subnet mask can be entered here.



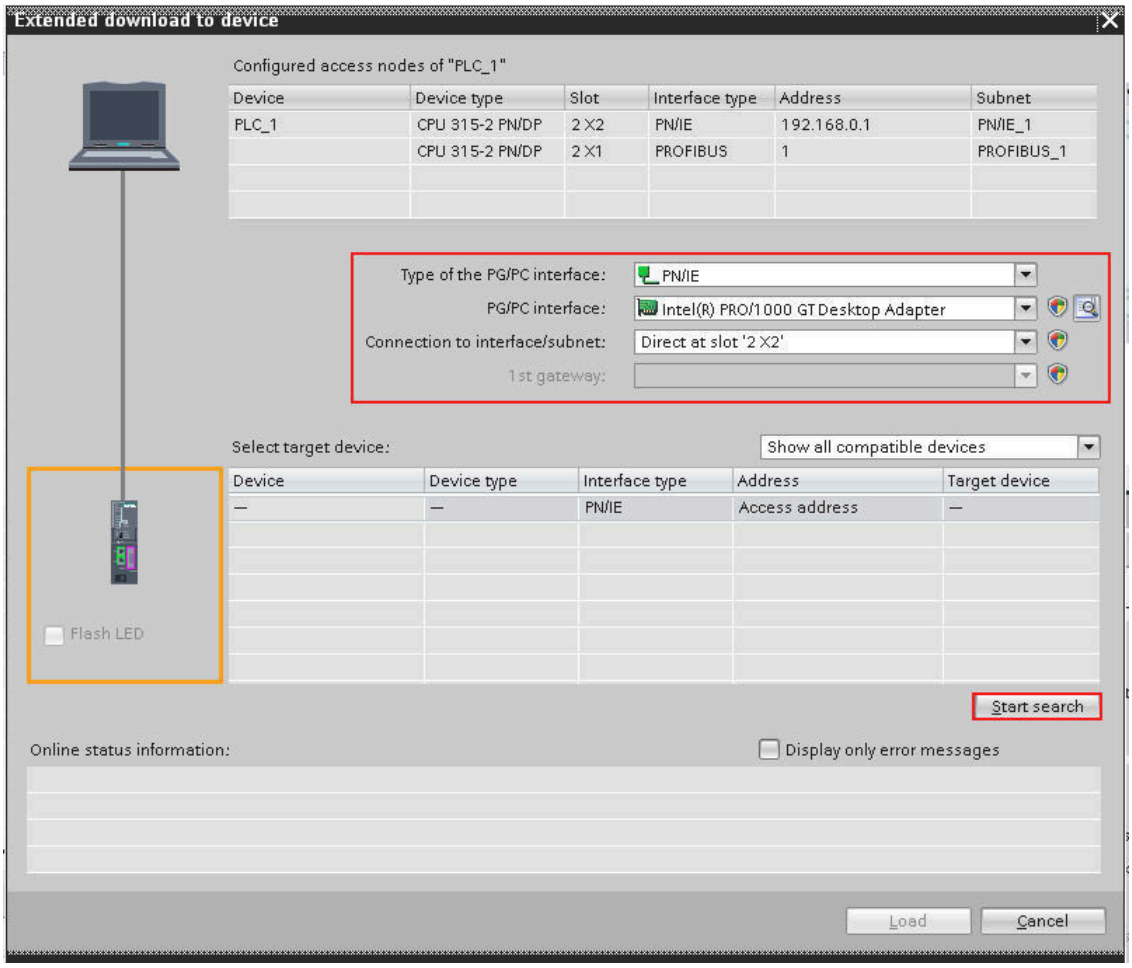
● Now the project can be compiled. To do this, select CPU "PLC_1[CPU 315-2 PN/DP]" in the **Project tree** view and button **Compile** in the toolbar.



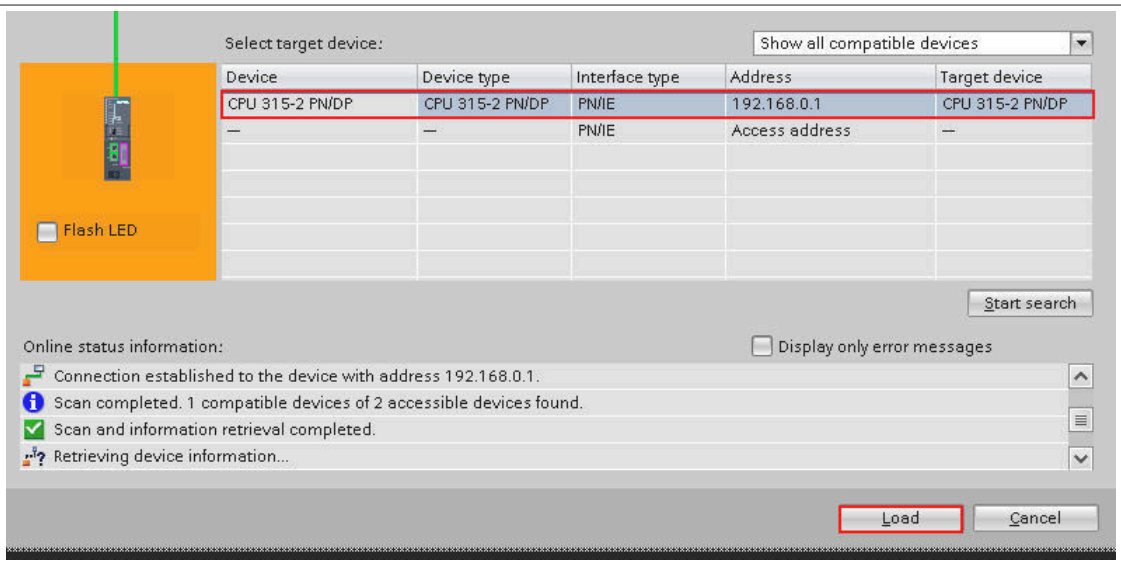
● After the project has been successfully compiled, it can be loaded onto the device. To do this, select button **Download to device** in the toolbar.



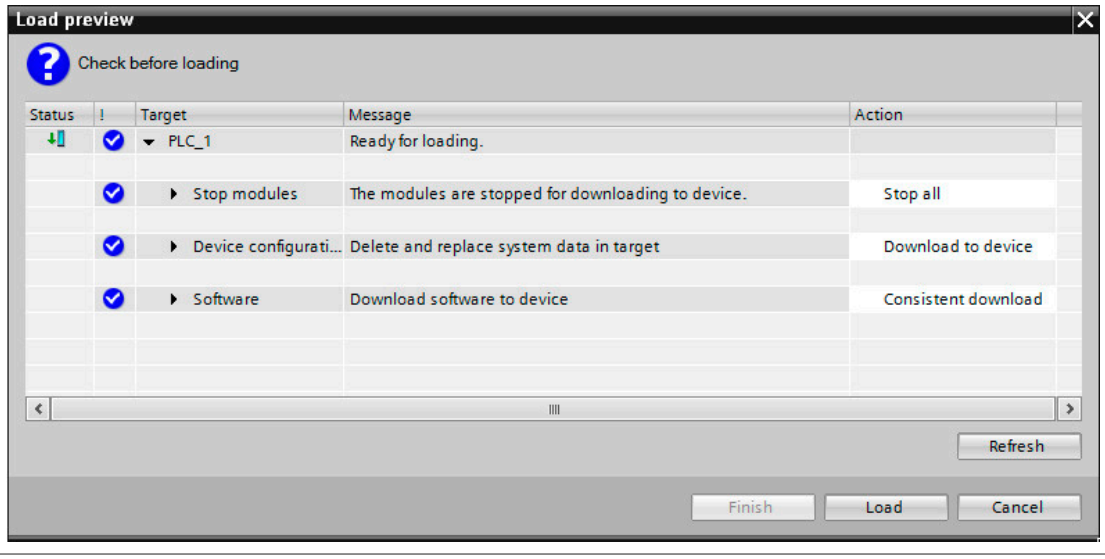
● A query dialog box opens in which the interface configuration is set.
With button **Start search**, the network is scanned for devices. If no devices are found, this indicates that an incorrect IP address was set in the CPU.



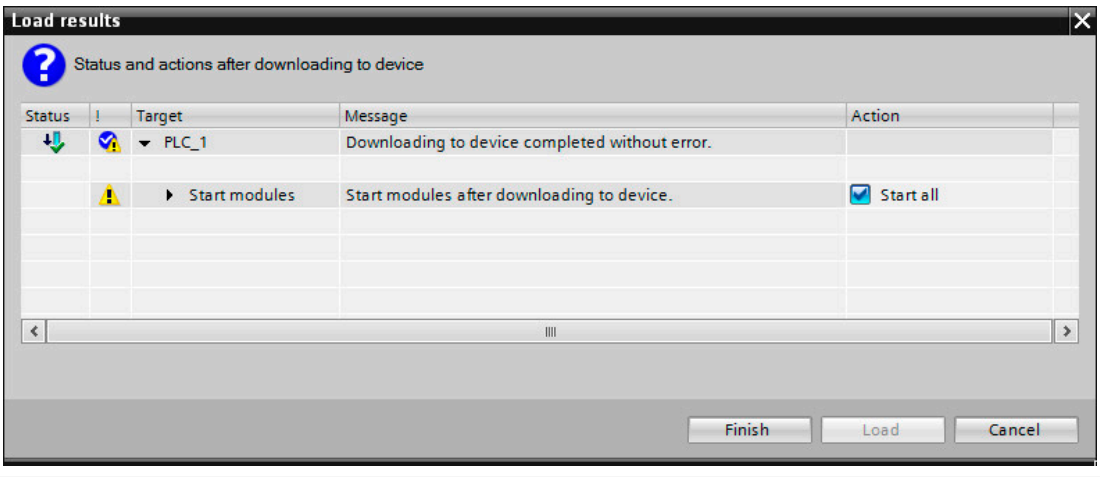
● If the search is successful, the devices found are listed under **Compatible devices in target subnet**. After selecting the CPU, the data can be loaded to the CPU with button **Load**.



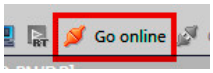
● Before loading, a notification window opens and lists a preview of all loading processes. This can be used to check whether the correct data is being transferred. The data is transferred after pressing **Load**.



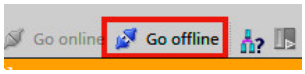
● The result of the loading process is listed and must be confirmed with **Finish**.



● Select button **Go online** to establish a connection to the CPU. The connection is established and, if configured correctly, the slave is set to state "Run".
In state "Run", no changes can be made to the configuration or application.



● With button **Go offline**, the connection to the CPU can be disconnected.



● The application can be started or stopped in the toolbar via buttons **Start CPU** and **Stop CPU**.



7 Register description

7.1 Structure of PROFIBUS data

Cyclic data from the PROFIBUS DP master is distributed between the connected X2X Link modules.

The position of individual I/O modules in the PROFIBUS data is determined by the configuration on the master. A module can occupy more or fewer bytes in the PROFIBUS data depending on the variant selected.

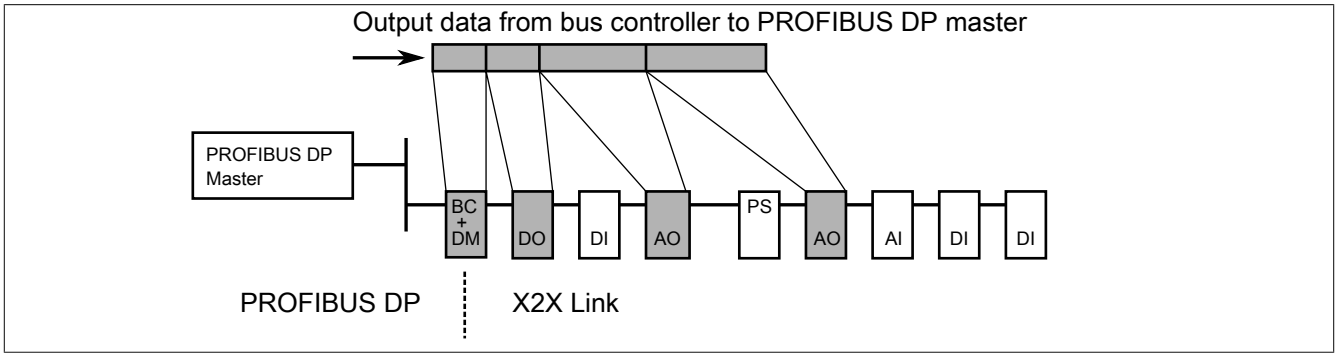


Figure 1: PROFIBUS DP output data

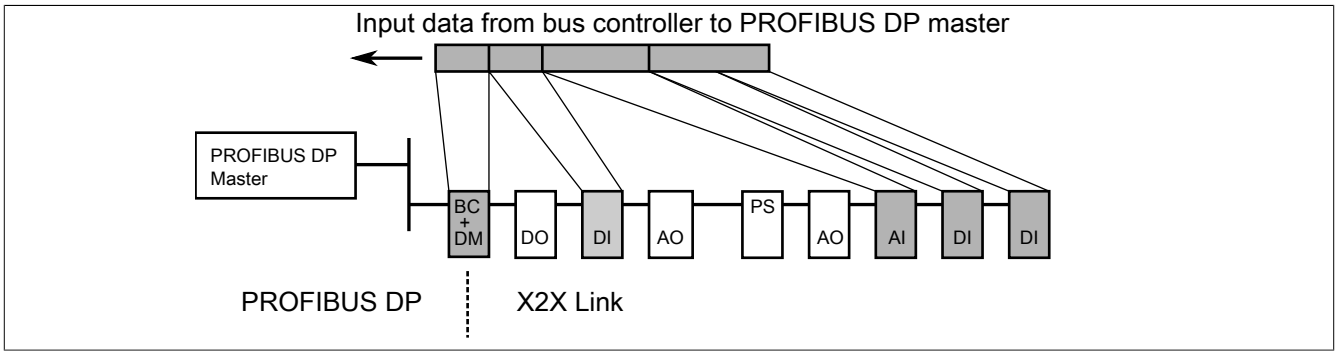


Figure 2: PROFIBUS DP input data

The number of required bytes and the position of the registers within a module are described on the following pages.

7.2 Module list

The following list includes all I/O modules which are supported by the current GSD version.

7.2.1 Additional information

Detailed information and technical data for the individual modules can be taken from the "X20 system user's manual" and the corresponding module data sheet. All documents can be found online at www.br-automation.com.

7.2.2 PROFIBUS GSD-function models

Some modules are listed with various configurations:

Module Cxy

x	Function
0	Standard
1 - 9	Extended function range

y	Function
1	Only necessary registers are contained in the cyclic data. • Module channels are configured in the engineering tool. • Status registers are partly transferred to the master as diagnostic information automatically.
2	If y=1, however, the status registers are also transferred in the cyclic data.
3	The configuration registers in the module are transferred in the cyclic data. It is not possible to configure the channels using dialog boxes. The user must configure the channels using the software in the CPU program. The structure of the respective configuration registers can be found in the user's manual for the I/O module.
4	Summary of 2 and 3

7.2.3 Overview of the terms used in the tables

Fields marked in gray represent cyclic input and output data. The following applies:

- Long Input/Output channel with a channel width of 4 byte
- Word Input/Output channel with a channel width of 2 byte
- Byte Input/Output channel with a channel width of 1 byte

Fields with footnotes describe module registers that are used for configuration and diagnostics data. This data is transferred acyclically. The column "Data bytes in DP frame" lists the sum of the cyclic input and output data.

7.3 X20 I/O system

7.3.1 Bus receivers/transmitters

7.3.1.1 X20BR9300 / X20BT9x00

Register	Name	Bytes	Module							
			X20BT9100-C01		X20BT9100-C02		X20BR9300-C01 X20BT9400-C01		X20BR9300-C02 X20BT9400-C02	
Input:										
0	Bus supply status	1			Byte				Byte	
2	Supply current	1							Byte	
4	Supply voltage	1			Byte				Byte	
Data bytes in DP frame			0 in	0 out	2 in	0 out	0 in	0 out	3 in	0 out

Bus supply status

The supply voltage and current of the module are monitored in this register.

Bit	Name	Value	Information
0	Bus supply	0	No error
		1	Bus supply warning for undervoltage (or overcurrent)
1	Reserved	0	
2	I/O supply	0	I/O supply above the warning threshold of 20.4 V
		1	I/O supply below the warning threshold of 20.4 V
3 - 7	Reserved	0	

Supply current

The bus supply current is indicated in this register.

Values	Information
0 to 255	X20BR9300: Resolution = 0.1 A X20BT9400: Resolution = 0.01 A

Supply voltage

The bus supply voltage is indicated in this register.

Values	Information
0 to 255	Resolution = 0.1 V

7.3.2 Power supply modules

7.3.2.1 X20PS21x0 / X20PS33x0 / X20PS940x

Register	Name	Bytes	Module							
			X20PS2100-C01 X20PS2110-C01 X20(c)PS9400-C01 X20PS9402-C01		X20PS2100-C02 X20PS2110-C02 X20(c)PS9400-C02 X20PS9402-C02		X20PS3300-C01 X20PS3310-C01		X20PS3300-C02 X20PS3310-C02	
Input:										
0	Bus supply status	1			Byte				Byte	
2	Supply current	1							Byte	
4	Supply voltage	1			Byte				Byte	
Data bytes in DP frame			0 in	0 out	2 in	0 out	0 in	0 out	3 in	0 out

Bus supply status

The supply voltage and current of the module are monitored in this register.

Bit	Name	Value	Information
0	Bus supply	0	No error
		1	Bus supply warning - Undervoltage (<4.7 V)
1	X20PS2110: Fuse Other modules: Reserved	0	Fuse OK or hardware revision <C0
		1	Fuse defective
2	I/O supply	0	I/O supply above the warning threshold of 20.4 V
		1	I/O supply below the warning threshold of 20.4 V
3 - 7	Reserved	0	

Supply current

The bus supply current is indicated in this register.

Values	Information
0 to 255	Resolution = 0.1 A

Supply voltage

The bus supply voltage is indicated in this register.

Values	Information
0 to 255	Resolution = 0.1 V

7.3.3 Digital input modules

7.3.3.1 X20DIx37x / X20DIx653 / X20DI0471 / X20DI6553

Register	Name	Bytes	Module							
			X20DI2371 X20DI2372 X20DI2653 X20(c)DI4371 X20DI4372 X20DI4653 X20DI6371 X20DI6372 X20DI6373 X20DI6553 X20DI8371 X20DID371		X20DI0471		X20DI6371-C11 X20DI6372-C11 X20DI6373-C11		X20(c)DI9371 X20DI9372 X20(c)DIF371	
Input:										
0	Digital inputs 1 - x	1	Byte		Byte		Byte		Byte	
1	Digital inputs 9 - x	1			Byte				Byte	
-	Filler byte	1					Byte			
Output:										
18	Input filter	1		1)	Byte	1)		1)		1)
Data bytes in DP frame			1 in	0 out	3 in	0 out	2 in	0 out	2 in	0 out

1) The register is transferred acyclically.

Digital inputs

This register is used to indicate the input state of the digital inputs. As a result, the input with the lowest channel number is located in the LSB; the bits of the inputs that are not present are 0.

Bit	Name	Value	Information
0	Channel 1 or 9	0 or 1	Input state - Digital input
...		...	
x	Channel 1 or 9 + x	0 or 1	Input state - Digital input

Input filter

The filter value can be configured in steps of 100 µs. It makes sense to enter values in steps of 2, however, since the input signals are sampled every 200 µs.

Values	Filter
0	No software filter
2	0.2 ms
...	...
250	25 ms - Higher values are limited to this value

Filler byte

GSD models **X20DI637x-C11** provide an extra input byte with zeros, unlike models **X20DI637x**. This supports master systems with word alignment.

7.3.3.2 X20DI2377

Register	Name	Bytes	Module X20DI2377	
Input:				
4	Counter 1	2	Word	
6	Counter 2	2	Word	
0	Digital inputs 1 - 2	1	Byte	
26	Input latch	1	Byte	
Output:				
18	Input filter	1		1)
20	Counter configuration 1	1		1)
22	Counter configuration 2	1		1)
28	Reset input latch	1		Byte
Data bytes in DP frame			6 in	1 out

1) The register is transferred acyclically.

Counter

This register displays the results of the individual counters. Event counter or gate measurement, depending on the operating mode. Only one of the two counters can be used for gate-time measurement.

Values
0 to 65535

Digital inputs

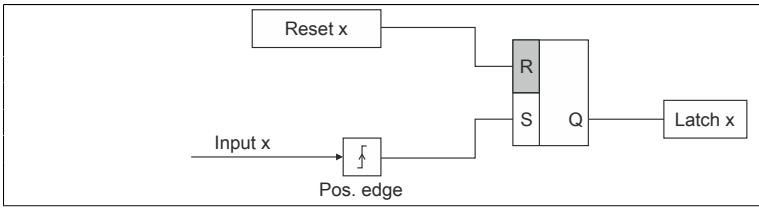
This register is used to indicate the input state of the digital inputs. As a result, the input with the lowest channel number is located in the LSB; the bits of the inputs that are not present are 0.

Bit	Name	Value	Information
0	Channel 1	0 or 1	Input state - Digital input
1	Channel 2	0 or 1	Input state - Digital input

Input latch

Using this function, the rising edges of the input signal can be latched with a resolution of 200 µs. With the "Acknowledge - input latch" function, the input latch is either reset or prevented from latching.

It works in the same way as a dominant reset RS flip-flop.



R	S	Q	Status
0	0	x	Do not change
0	1	1	Set
1	0	0	Reset
1	1	0	Reset

Bit	Name	Value	Information
0	Channel 1	0 or 1	Input state of digital input 1 after expiration of the delay time
1	Channel 2	0 or 1	Input state of digital input 2 after expiration of the delay time
2 - 7	Reserved	-	

Input filter

The filter value can be configured in steps of 100 µs. It makes sense to enter values in steps of 2, however, since the input signals are sampled every 200 µs.

Values	Filter
0	No software filter
2	0.2 ms
...	...
250	25 ms - Higher values are limited to this value

Counter configuration

This register can be used to configure the individual counters.

Bit	Name	Value	Information
0 - 3	Counter frequency	0	48 MHz (only with gate measurement)
		1	3 MHz (only with gate measurement)
		1	**Event counter** via software (only in event counter operation)
		2	187.5 kHz (only with gate measurement)
		3	24 MHz (only with gate measurement)
		4	12 MHz (only with gate measurement)
		5	6 MHz (only with gate measurement)
		6	1.5 MHz (only with gate measurement)
		7	750 kHz (only with gate measurement)
		8	375 kHz (only with gate measurement)
4	Reserved	0	
5	Reset counter	0	No influence on the counter
		1	Clear counter (at rising edge)
6 - 7	Type of measurement	0	Event counter measurement
		1	Gate measurement

Reset input latch

Used to reset the corresponding channels and prevent latching. See diagram: Input latch.

Bit	Name	Value	Information
0	Acknowledge latch 1	0	No influence on the latch status
		1	Resets the latch status
1	Acknowledge latch 2	0	No influence on the latch status
		1	Resets the latch status
2 - 7	Reserved	-	

7.3.3.3 X20DI4375

Register	Name	Bytes	Module X20DI4375	
Input:				
2305	Digital inputs	1	Byte	
2307	Short circuit monitoring of channels	1	Byte	
2309	Open circuit monitoring of channels	1	Byte	
2311	Voltage monitoring of channels	1	Byte	
2313	Error monitoring of channels	1	Byte	
Output:				
2050	Configuration of line status monitoring	2		1)
2053	Input filter	1		1)
Data bytes in DP frame			5 in	0 out

1) The register is transferred acyclically.

Digital inputs

This register indicates the input state and status of digital inputs 1 to 4.

Bit	Name	Value	Information
0	Input channel 1	0 or 1	Input state - Digital input 1
...		...	
3	Input channel 4	0 or 1	Input state - Digital input 4
4	State of input channel 1	0	No error
		1	Short circuit, open circuit, sensor monitoring error or other channel error
...		...	
7	State of input channel 4	0	No error
		1	Short circuit, open circuit, sensor monitoring error or other channel error

Short circuit monitoring of channels

This register indicates whether a short circuit has occurred on the individual channels.

Bit	Name	Value	Information
0	Channel 1	0	No error
		1	Short circuit on channel 1
...		...	
3	Channel 4	0	No error
		1	Short circuit on channel 4
4 - 7	Reserved	-	

Open circuit monitoring of channels

This register indicates whether an open circuit has occurred on the individual channels.

Bit	Name	Value	Information
0	Channel 1	0	No error
		1	Open circuit on channel 1
...		...	
3	Channel 4	0	No error
		1	Open circuit on channel 4
4 - 7	Reserved	-	

Voltage monitoring of channels

This register monitors the voltage supply on the individual channels.

Bit	Name	Value	Information
0	Channel 1	0	No error
		1	Sensor supply error on channel 1
...		...	
3	Channel 4	0	No error
		1	Sensor supply error on channel 4
4 - 7	Reserved	-	

Error monitoring of channels

This register indicates whether any other errors have occurred on the individual channels.

Data type	Values	Information
USINT	0 to 15	Packed inputs = On
	See bit structure.	Packed inputs = Off or Function model <> 0 - Standard

Bit	Name	Value	Information
0	Channel 1	0	No error
		1	Other error on channel 1
...		...	
3	Channel 4	0	No error
		1	Other error on channel 4
4 - 7	Reserved	-	

Configuration of line status monitoring

This register is used to configure short circuit monitoring and line status monitoring on the inputs.

Bit	Name	Value	Information
0 - 3	Channel configuration - Channel 1	0	Standard
		1	Serial/Parallel: R-1k in series with (R-10k parallel to the switch)
		2	Parallel/Serial: R-10k parallel to (R-1k in series with switch)
		3	Parallel: R-10k parallel to switch
		4	Serial: R-1k in series with switch
		5 to 15	Inactive
4 - 7	Channel configuration - Channel 2	0 to 15	See Channel configuration - Channel 1
8 - 11	Channel configuration - Channel 3	0 to 15	See Channel configuration - Channel 1
12 - 15	Channel configuration - Channel 4	0 to 15	See Channel configuration - Channel 1

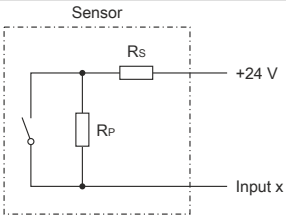
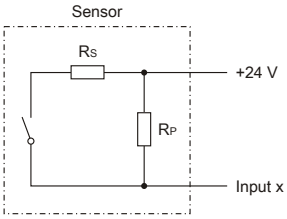
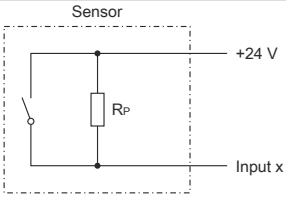
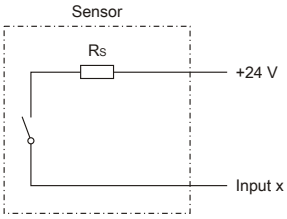
The name R-1k indicates a resistance in the permitted range of 1000 Ohm to 2000 Ohm with an accuracy of 10%.

The name R-10k indicates a resistance in the permitted range of 10000 Ohm to 20000 Ohm with an accuracy of 10%.

Information:

Inputs that are not being used should be set to the type "Standard" or "Serial" to prevent mistakes.

Configuration of line status monitoring

Value	Configuration	Diagram	Information
0	**Standard**		Short-circuit detection and line break monitoring is not possible when using this configuration.
1	**Serial/parallel**		Short-circuit detection and line break monitoring is possible with this configuration.
2	**Parallel/serial**		Short-circuit detection and line break monitoring is possible with this configuration.
3	**Parallel**		This configuration allows line break monitoring. Short-circuit detection is not possible when using this configuration.
4	**Serial**		This configuration allows short circuit detection. Line break monitoring is not possible when using this configuration.

Input filter

The filter value can be configured in steps of 100 µs. It makes sense to enter values in steps of 2, however, since the input signals are sampled every 200 µs.

Values	Filter
0	No software filter
2	0.2 ms
...	...
250	25 ms - Higher values are limited to this value

7.3.3.4 X20DI4760

Register	Name	Bytes	Module			
			X20DI4760-C02		X20DI4760-C12	
Input:						
0	Digital inputs 1 - 4	1	Byte		Byte	
30	Input status[1)]	1	Byte		Byte	
4	Edge counters Channel 1	1			Byte	
6	Edge counters Channel 2	1			Byte	
8	Edge counters Channel 3	1			Byte	
10	Edge counters Channel 4	1			Byte	
Output:						
16	Channel selection	1	[2)]		[2)]	
Data bytes in DP frame			2 in	0 out	6 in	0 out

1) A portion of the diagnostics information is automatically sent to the PROFIBUS DP master. See Input status
2) The register can be modified in the parameter dialog box for the I/O module and is transferred acyclically.

Digital inputs

This register is used to indicate the input state of the digital inputs. As a result, the input with the lowest channel number is located in the LSB; the bits of the inputs that are not present are 0.

Bit	Name	Value	Information
0	Channel 1	0 or 1	Input state - Digital input 1
...		...	
3	Channel 4	0 or 1	Input state - Digital input 4

Input status

This register indicates whether an open line or overflow has occurred on the individual channels.

Overload - Channels 1 - 4 are automatically sent to the PROFIBUS DP master. Open line - Channels 1 - 4 must be evaluated via the application

Bit	Name	Value	Information
0	Overload - Channel 1	0	No error
		1	Overload
...		...	
3	Overload - Channel 4	0	No error
		1	Overload
4	Open line - Channel 1	0	No error
		1	Open line
...		...	
7	Open line - Channel 4	0	No error
		1	Open line

Edge counters

These registers cyclically count the rising edges on the individual channels.

Values	Information
0 to 255	Rising edge counter on channel, cyclic

Channel selection

Information:

Revision A5 or higher of the I/O module is required.

This register can be used to (de)activate individual channels or just their status responses.

Bit	Name	Value	Information
0	Channel 1	0	Channel enabled
		1	Channel disabled
...		...	
3	Channel 4	0	Channel enabled
		1	Channel disabled
4	Status message - Channel 1	0	Status message activated
		1	Status message deactivated
...		...	
7	Status message - Channel 4	0	Status message activated
		1	Status message deactivated

7.3.4 Digital output modules

7.3.4.1 X20DOx32x / X20DOx33x

Register	Name	Bytes	Module							
			X20DO2321 X20DO2322 X20DO4321 X20DO4322 X20DO4331 X20(c)DO4332 X20DO6321 X20DO6322 X20DO8322 X20DO8331 X20DO8332 X20DOD322		X20(c)DO9321 X20DO9322 X20DOF322		X20DO4321-C01 X20DO4322-C01 X20DO4331-C01 X20(c)DO4332-C01 X20DO6321-C01 X20DO6322-C01 X20DO8322-C01 X20DO8331-C01 X20DO8332-C01		X20DO9321-C01 X20DO9322-C01	
Input:										
30	Status of the outputs 1 - x[1)]	1	Byte		Byte					
31	Status of the outputs 9 - x[1)]	1			Byte					
Output:										
2	Digital outputs 1 - x	1		Byte		Byte		Byte		Byte
3	Digital outputs 9 - x	1				Byte				Byte
Data bytes in DP frame			1 in	1 out	2 in	2 out	0 in	1 out	0 in	2 out

1) Diagnostics information is automatically sent to the PROFIBUS DP master.

Status of the outputs

This register is used to indicate the status of the digital outputs.

GSD models **X20 DO xxxx-C01** do not return a status byte unlike **X20 DO xxxx**. The **-C01** models can be used in the event that this data is not required as cyclic information. However, if an error does occur then a diagnostics message will still be sent.

Bit	Name	Value	Information
0	Channel 1 (or 9)	0	No error
		1	Short circuit or overload
...		...	
x	Channel 1 (or 9) + x	0	No error
		1	Short circuit or overload

Digital outputs

This register is used to indicate the output status of the digital outputs. As a result, the output with the lowest channel number is located in the LSB; the bits of the outputs that are not present are ignored by the module.

Bit	Name	Value	Information
0	Channel 1 (or 9)	0	Digital output reset
		1	Digital output set
...		...	
x	Channel 1 (or 9) + x	0	Digital output reset
		1	Digital output set

7.3.4.2 X20DOx529 / X20DOx649

Register	Name	Bytes	Module X20DO2649 X20DO4529 X20DO4649 X20DO6529	
Output:				
2	Digital outputs 1 - x	1		Byte
Data bytes in DP frame			0 in	1 out

Digital outputs

This register is used to indicate the output status of the digital outputs. As a result, the output with the lowest channel number is located in the LSB; the bits of the outputs that are not present are ignored by the module.

Bit	Name	Value	Information
0	Channel 1	0	Digital output reset
		1	Digital output set
...		...	
x	Channel x	0	Digital output reset
		1	Digital output set

7.3.4.3 X20DOx623

Register	Name	Bytes	Module							
			X20DO2623		X20DO2623-C01		X20DO4623		X20DO4623-C01	
Input:										
30	Status of the outputs 1 - x	1	Byte		Byte		Byte		Byte	
Output:										
2	Digital outputs 1 - x	1		Byte		Byte		Byte		Byte
4	Analog output 1	1		Byte				Byte		
6	Analog output 2	1		Byte				Byte		
8	Analog output 3	1						Byte		
10	Analog output 4	1						Byte		
28	Output configuration	1		1)				1)		
Data bytes in DP frame			1 in	3 out	1 in	1 out	1 in	5 out	1 in	1 out

1) The register can be modified in the parameter dialog box for the I/O module and is transferred acyclically.

Status of the outputs

Zero-crossing detection works with a fixed filter time of 1 ms and a sampling frequency of 10 kHz. When a missing or too short period is detected, control is switched off until at least 2 periods are detected correctly, and the status flag is set accordingly. Control takes place with a delay of 2 ms before the negative half-wave until correct detection of the next zero crossing or another error. This is normally at least one complete wave.

Monitoring is activated at the first zero crossover after being switched on.

Bit	Name	Value	Information
0	Zero crossing[1)]	0	Signal during the negative half-wave
		1	Signal during the positive half-wave
1 - 3	Reserved	0	
4	Zero crossing error	0	No error
		1	Zero crossover failed
5 - 7	Reserved	0	

1) Value is valid if no error has occurred (zero crossing error = 0)

Digital outputs

This register is used to indicate the output status of the digital outputs. As a result, the output with the lowest channel number is located in the LSB; the bits of the outputs that are not present are ignored by the module.

Bit	Name	Value	Information
0	Channel 1	0	Digital output reset
		1	Digital output set
...		...	
x	Channel x	0	Digital output reset
		1	Digital output set

Analog output

The output value is transferred to the control switch synchronously with the connected network according to the ignition pattern table. The analog value is output with a resolution of ~4% over a duration of 24 complete waves. Values > 96% result in full control. Changes to the output value within an interval are applied after the next zero crossover.

Values	Information
0 to 100	Output value for the respective channel in percent
> 100	Corresponds to 100%

Information:

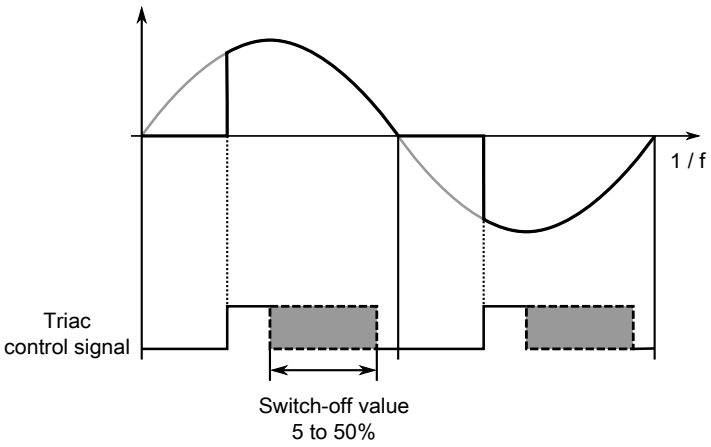
The states in these registers are only applied when the channels are set to ANALOG in the "Output configuration" register.

Off time

This value defines how far in front of the zero crossing the internal control signal for the TRIAC is switched off. Increasing this value may be necessary in order to prevent unwanted firing of the TRIAC in the event of a slight disturbance in the mains frequency.

With smaller loads, it is important to ensure that this switch off value is not set to large (too early) to prevent switching off prematurely.

The triac can of course only be fired before the set switch-off time.



Values	Function
5 to 50	Switch-off time in %

Output configuration

Allows individual configuration of the exit channels either to "digital" or "analog". Depending on the setting, the corresponding digital or analog outputs must be written.

Bit	Name	Value	Information
0	Channel 1	0	Digital register is used
		1	Analog register is used
1	Channel 2	0	Digital register is used
		1	Analog register is used
2	Channel 3 (only X20DO4xxx)	0	Digital register is used
		1	Analog register is used
3	Channel 4 (only X20DO4xxx)	0	Digital register is used
		1	Analog register is used
2 or 4 - 7	Reserved	0	

7.3.4.4 X20DO6325

Register	Name	Bytes	Module X20DO6325	
Input:				
28	Short circuit to GND and overtemperature	1	Byte	
29	Short circuit to voltage	1	Byte	
30	Open circuit	1	Byte	
31	Cumulative status	1	Byte	
Output:				
2	Digital outputs	1		Byte
4	Enabling the status LED	1		1)
Data bytes in DP frame			4 in	1 out

1) The register is transferred acyclically.

Short circuit to GND and overtemperature

In this register, a short circuit or overtemperature error is indicated by the corresponding channel bit being set. It is not possible to differentiate between short circuit to GND and overload/overtemperature.

Bit	Name	Value	Information
0	Channel 1	0	No error
		1	Channel 1: Short circuit or overload
...		...	
5	Channel 6	0	No error
		1	Channel 6: Short circuit or overload
6 - 7	Reserved	0	

Short circuit to voltage

In this register, a short circuit is indicated by the corresponding channel bit being set.

Bit	Name	Value	Information
0	Channel 1	0	No error
		1	Channel 1: Short circuit to voltage
...		...	
5	Channel 6	0	No error
		1	Channel 6: Short circuit to voltage
6 - 7	Reserved	0	

Open circuit

In this register, an open circuit is indicated by the corresponding channel bit being set.

Bit	Name	Value	Information
0	Channel 1	0	No error
		1	Channel 1: Open circuit
...		...	
5	Channel 6	0	No error
		1	Channel 6: Open circuit
6 - 7	Reserved	0	

Cumulative status

Every error pending in the other status registers is also indicated in this register. This provides an easy way to check whether any errors have occurred.
If the I/O power supply fails, Bit 7 is set and all status bits in the other status registers are reset to 0.

Bit	Name	Value	Information
0	Channel 1	0	No error
		1	Channel 1: Error occurred
...		...	
5	Channel 6	0	No error
		1	Channel 6: Error occurred
6	Reserved	0	
7	Status of the supply voltage	0	No error
		1	Pending supply voltage error

Digital outputs

This register is used to indicate the output status of the digital outputs. As a result, the output with the lowest channel number is located in the LSB; the bits of the outputs that are not present are ignored by the module.

Bit	Name	Value	Information
0	Channel 1	0	Digital output reset
		1	Digital output set
...		...	
5	Channel 6	0	Digital output reset
		1	Digital output set

Enabling the status LED

For each output there is a corresponding enable bit. In this register, the bit can be set to define whether or not the status LED should be used to indicate an open circuit error. This allows the LED to be disabled for unused channels. In the bus controller function model, the default value is 0xBF.

Bit	Name	Value	Information
0	Channel 1	0	Open circuit indicator 01 disabled
		1	Open circuit indicator 01 enabled
...		...	
5	Channel 6	0	Open circuit indicator 06 disabled
		1	Open circuit indicator 06 enabled
6	Reserved	0	
7	Supply voltage	0	No error status indicators
		1	Monitor supply voltage

7.3.4.5 X20DOx633

Register	Name	Bytes	Module							
			X20DO2633		X20DO2633-C01		X20DO4633		X20DO4633-C01	
Input:										
30	Status of the outputs 1 - x	1	Byte		Byte		Byte		Byte	
Output:										
2	Digital outputs 1 - x	1		Byte		Byte				Byte
4	Analog output 1	1		Byte				Byte		
6	Analog output 2	1		Byte				Byte		
8	Analog output 3	1		Byte				Byte		
10	Analog output 4	1		Byte				Byte		
20	Off time 1	1						1)		1)
22	Off time 2	1						1)		1)
24	Off time 3	1						1)		1)
26	Off time 4	1						1)		1)
28	Output configuration	1		1)				1)		1)
Data bytes in DP frame			1 in	5 out	1 in	1 out	1 in	4 out	1 in	1 out

1) The register can be modified in the parameter dialog box for the I/O module and is transferred acyclically.

Status of the outputs

The operating status of the outputs is mapped in this register.

In order to do determine the current flow status, the system checks if there is a neutral connection from the output via the consumer shortly before each triac firing.

Bit	Name	Value	Information
0	Current flow status 1	0	Current flow on activated output 1
		1	No current flow on activated output 1
1	Current flow status 2	0	Current flow on activated output 2
		1	No current flow on activated output 2
2	Current flow status 3 (only X20DO4633)	0	Current flow on activated output 3
		1	No current flow on activated output 3
3	Current flow status 4 (only X20DO4633)	0	Current flow on activated output 4
		1	No current flow on activated output 4
4	Zero crossing	0	Zero cross signal during the negative half-wave
		1	Zero cross signal during the positive half-wave
5 - 6	Reserved	-	
7	Zero crossing status	0	Zero cross signal OK
		1	Zero cross signal has dropped out

Digital outputs

This register is used to indicate the output status of the digital outputs. As a result, the output with the lowest channel number is located in the LSB; the bits of the outputs that are not present are ignored by the module.

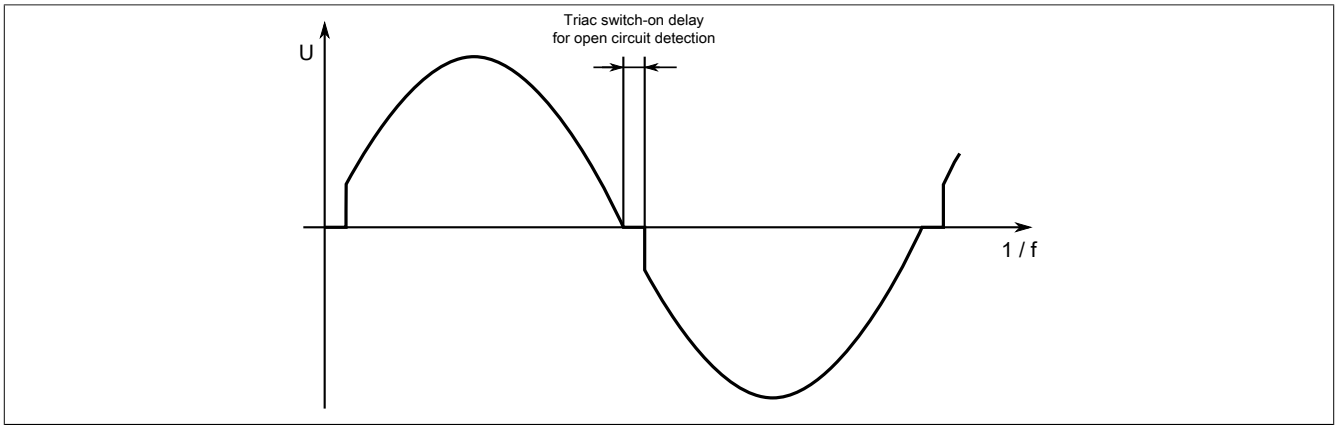
Bit	Name	Value	Information
0	Channel 1	0	Digital output reset
		1	Digital output set
...		...	
x	Channel x	0	Digital output reset
		1	Digital output set

Analog output

The output value of the outputs defined as analog outputs (unit percent) is switched through to the control ports in sync with power mains. The analog value is output to the TRIAC control port in the range between (output value > SwitchOffValue) and (output value <= 95%) with a resolution of 1%.

A short triac turn-on delay is required for open line detection. Therefore even with output values >= 96%, there is a small pause in control.

Changes to the output value are applied at the next positive half-wave



Values	Information
0 to 100	Output value for the respective channel in percent
> 100	Corresponds to 100%

Information:

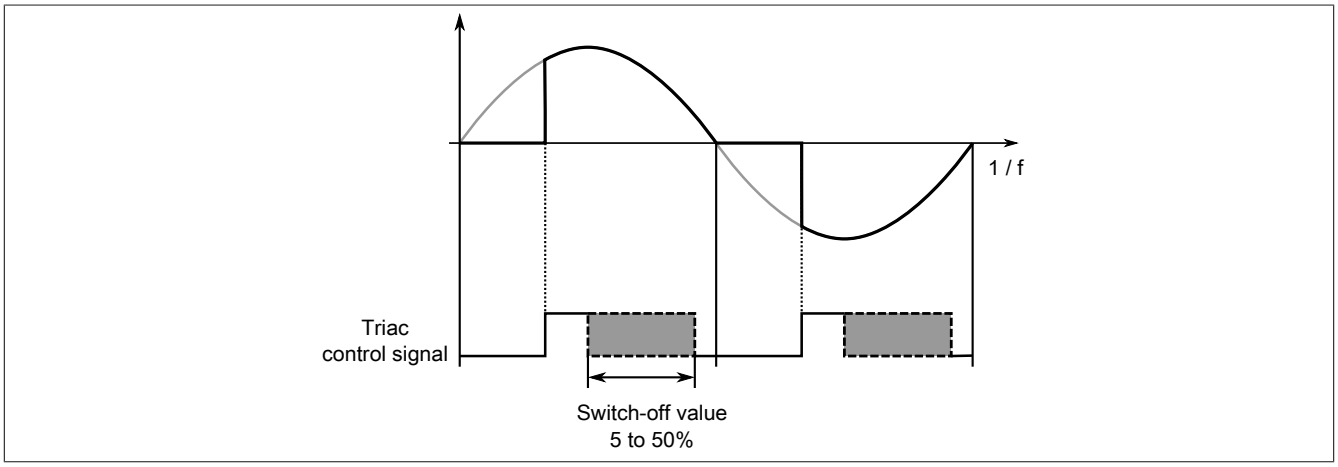
The commutation angle for phase angle control set in these registers are only applied when the channels are set to ANALOG in the Output configuration register.

Off time

This value defines how far in front of the zero crossing the internal control signal for the TRIAC is switched off. Increasing this value may be necessary in order to prevent unwanted firing of the TRIAC in the event of a slight disturbance in the mains frequency.

With smaller loads, it is important to ensure that this switch off value is not set to large (too early) to prevent switching off prematurely.

The triac can of course only be fired before the set switch-off time.



Values	Function
5 to 50	Switch-off time in %

Output configuration

This allows the operating mode to be changed from full-wave control to half-wave control for each channel.

Bit	Name	Value	Information
0	Channel 1: Digital / Analog output	0	Output channel 1 is defined as a digital output. The output status is defined in bit 0 of the Digital outputs register.
		1	Output channel 1 is defined as an analog output. The output status is defined in the Analog output register.
...		...	
3	Channel 4: Digital / Analog output	0	Output channel 4 is defined as a digital output. The output status is defined in bit 1 of the Digital outputs register.
		1	Output channel 2 is defined as an analog output. The output status is defined in the Analog output register.
4	Channel 1: Full-wave / half-wave control	0	Full-wave control on output channel 1
		1	Negative half-wave on output channel 1 is suppressed.
...		...	
7	Channel 4: Full-wave / half-wave control	0	Full-wave control on output channel 4
		1	Negative half-wave on output channel 4 is suppressed.

7.3.4.6 X20DO6639

Register	Name	Bytes	Module X20DO6639	
Output:				
0	Digital outputs 1 - 6	1		Byte
Data bytes in DP frame			0 in	1 out

Support with firmware version ≥ V1.43

Digital outputs

This register is used to indicate the output status of the digital outputs. As a result, the output with the lowest channel number is located in the LSB; the bits of the outputs that are not present are ignored by the module.

Bit	Name	Value	Information
0	Channel 1	0	Digital output reset
		1	Digital output set
...		...	
5	Channel 6	0	Digital output reset
		1	Digital output set

7.3.4.7 X20DO8323

Register	Name	Bytes	Module X20DO8323	
Input:				
0	Digital inputs 1 - 8	1	Byte	
2	Digital outputs 1 - 8	1	Byte	
4	Switching between digital inputs/outputs	1	Byte	
Output:				
30	Status of the outputs	1		Byte
31	Cumulative status	1		Byte
Data bytes in DP frame			3 in	2 out

Support with firmware version ≥ V1.43

Digital inputs

This register is used to indicate the input state of digital inputs 1 to 8.

The status of the digital inputs is read with a minimum update rate of 5 to 8 ms according to the digital output status sample rate.

Bit	Name	Value	Information
0	Input channel 1	0 or 1	Input state - Digital input 1
...		...	
7	Input channel 8	0 or 1	Input state - Digital input 8

Digital outputs

This register is used to indicate the output status of the digital outputs. As a result, the output with the lowest channel number is located in the LSB; the bits of the outputs that are not present are ignored by the module.

Bit	Name	Value	Information
0	Channel 1	0	Digital output reset
		1	Digital output set
...		...	
7	Channel 8	0	Digital output reset
		1	Digital output set

Switching between digital inputs/outputs

Each channel can be set as either an input or output using the corresponding switching bit. Clearing this bit switches to tristate mode.

Bit	Name	Value	Information
0	Channel 1	0	Used as an input
		1	Used as an output
...		...	
7	Channel 8	0	Used as an input
		1	Used as an output

Status of the outputs

This register is used to indicate the status of the digital outputs.

Bit	Name	Value	Information
0	Channel 1	0	No error
		1	Short circuit or overload
...		...	
7	Channel 8	0	No error
		1	Short circuit or overload

Cumulative status

The state of output monitoring and the voltage supply for all outputs are collected and mapped to this register.

Bit	Name	Value	Information
0	Output monitoring	0	No output monitoring
		1	Output monitoring active for at least one channel
1 - 3	Reserved	0	
4	Supply voltage too low	0	No error
		1	Supply voltage too low (≤11.5 VDC)
5	Supply voltage too high	0	No error
		1	Supply voltage too high (>30 VDC)
6 - 7	Reserved	0	

7.3.5 Digital mixed modules

7.3.5.1 X20DM9324

Register	Name	Bytes	Module X20DM9324	
Input:				
0	Digital inputs 1 - 8	1	Byte	
30	Status of the outputs 1 - 4[1)]	1		
Output:				
2	Digital outputs 1 - 4	1		Byte
18	Input filter	1		[2)]
Data bytes in DP frame			1 in	1 out

1) Diagnostics information is automatically sent to the PROFIBUS DP master.
2) The register can be modified in the parameter dialog box for the I/O module and is transferred acyclically.

Digital inputs

This register is used to indicate the input state of the digital inputs. As a result, the input with the lowest channel number is located in the LSB; the bits of the inputs that are not present are 0.

Bit	Name	Value	Information
0	Channel 1	0 or 1	Input state - Digital input
...		...	
7	Channel 8	0 or 1	Input state - Digital input

Status of the outputs

This register is used to indicate the status of the digital outputs.

Bit	Name	Value	Information
0	Channel 1	0	No error
		1	Short circuit or overload
...		...	
3	Channel 4	0	No error
		1	Short circuit or overload

Digital outputs

This register is used to indicate the output status of the digital outputs. As a result, the output with the lowest channel number is located in the LSB; the bits of the outputs that are not present are ignored by the module.

Bit	Name	Value	Information
0	Channel 1	0	Digital output reset
		1	Digital output set
...		...	
3	Channel 4	0	Digital output reset
		1	Digital output set

Input filter

The filter value can be configured in steps of 100 µs. It makes sense to enter values in steps of 2, however, since the input signals are sampled every 200 µs.

Values	Filter
0	No software filter
2	0.2 ms
...	...
250	25 ms - Higher values are limited to this value

7.3.6 Analog input modules

7.3.6.1 X20AI1744

Register	Name	Bytes	Module X20AI1744-C03 X20AI1744-3-C03	
Input:				
4	Analog input	4	Long	
2	**HI:** Reserved **LO:** A/D converter status	2	Word	
Output:				
16	A/D configuration	1		Byte
Data bytes in DP frame			6 in	1 out

Analog input

This register contains the raw value determined by the A/D converter for the full-bridge strain gauge with 24-bit resolution.

Values	Information
0x007FFFFF to 0xFF800001	Valid value range
0x007FFFFF	Overrun
0xFF800001	Underflow
0xFF800000	Invalid value

Effective resolution

In principle, the effective resolution of the A/D converter is dependent on the data rate and the measurement range (see Effective resolution of the A/D converter).

The following table shows how the effective resolution (in bits), or the effective value range of the strain gauge value depend on the module configuration (data rate, measurement area).

	Measurement range							
	±16 mV/V		±8 mV/V		±4 mV/V		±2 mV/V	
Data rate f_{DATA} [Hz]	Bits	Range of values	Bits	Range of values	Bits	Range of values	Bits	Range of values
2.5	21.3	±1,290,000	20.8	±912,000	19.7	±425,000	18.7	±212,000
5	20.7	±851,000	20.3	±645,000	19.3	±322,000	18.3	±161,000
10	20.4	±691,000	19.9	±490,000	18.9	±244,000	17.9	±122,000
15	20.1	±562,000	19.3	±320,000	18.7	±212,000	17.7	±106,000
25	19.7	±425,000	19.2	±301,000	18.5	±185,000	17.5	±92,000
30	19.6	±397,000	19.0	±262,000	18.1	±140,000	17.1	±72,000
50	19.4	±346,000	18.8	±230,000	17.9	±122,000	16.9	±61,000
60	19.3	±320,000	18.8	±230,000	17.8	±114,000	16.8	±57,000
100	19.1	±280,000	18.5	±185,000	17.4	±86,000	16.4	±43,000
500	18.0	±130,000	17.3	±80,000	16.3	±40,000	15.3	±20,000
1000	17.2	±75,000	16.5	±46,000	15.6	±25,000	14.6	±12,000
2000	16.6	±49,600	16.1	±35,000	15.3	±20,000	14.3	±10,000
3750	16.2	±37,600	15.7	±26,600	14.7	±13,000	13.7	±6,600
7500	15.8	±28,500	15.3	±20,200	14.4	±10,800	13.4	±5,400

Table 5: Effective resolution of the strain gauge value in bits for the measurement range 2 to 16 mV/V

	Measurement range							
	±256 mV/V		±128 mV/V		±64 mV/V		±32 mV/V	
Data rate f_{DATA} [Hz]	Bits	Range of values	Bits	Range of values	Bits	Range of values	Bits	Range of values
2.5	23	±4,194,000	22.6	±3,179,000	22.1	±2,248,000	21.7	±1,703,000
5	22.3	±2,582,000	22.4	±2,767,000	21.9	±1,957,000	21.3	±1,291,000
10	22.3	±2,582,000	22	±2,097,000	21.6	±1,589,000	21	±1,049,000
15	22	±2,097,000	21.7	±1,703,000	21.3	±1,291,000	20.7	±852,000
25	21.7	±1,703,000	21.4	±1,384,000	21.1	±1,124,000	20.5	±741,000
30	21.8	±1,826,000	21.3	±1,291,000	20.8	±913,000	20.4	±692,000
50	21.3	±1,291,000	21.1	±1,124,000	20.4	±692,000	19.9	±489,000
60	21.3	±1,291,000	20.9	±978,000	20.5	±741,000	19.8	±456,000
100	20.9	±978,000	20.7	±852,000	20.2	±602,000	19.6	±397,000
500	20.1	±562,000	19.6	±397,000	19.1	±281,000	18.6	±199,000
1000	19	±262,000	18.6	±199,000	18.1	±140,000	17.5	±93,000
2000	18.5	±185,000	18.1	±140,000	17.8	±114,000	17	±66,000
3750	18.1	±140,000	17.8	±114,000	17.3	±81,000	16.6	±50,000
7500	17.7	±106,000	17.3	±81,000	16.9	±61,000	16.2	±38,000

Table 6: Effective resolution of the strain gauge value in bits for the measurement range 32 to 256 mV/V

Effective resolution of the A/D converter

The AD converter on the AI1744 provides a 24 bit measurement value. However, the actual attainable noise-free resolution is always less than 24 bit. This "effective resolution" depends on the data rate and measurement range.

Example:

Because of the conversion method, a data rate of 2.5 Hz and a specified measurement area of 2 mV/V result in an effective resolution of 18.7 bits:

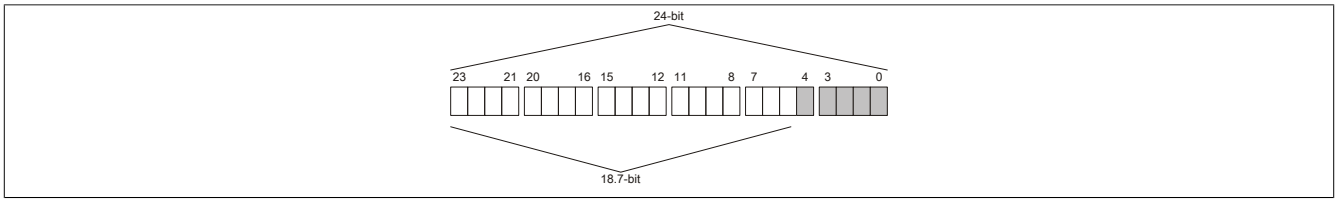


Figure 3: Example for the effective resolution of the AD converter

The low-order bits (grayed out) contain only noise instead of valid values and must therefore not be evaluated.

A/D converter status

The current state of the module is indicated in this register.

Bit	Description	Value	Information
0	A/D converter value	0	Valid A/D converter value
		1	Invalid A/D converter value
1	Line monitoring	0	OK
		1	Open line
2	Only valid in synchronous mode	0	A/D converter runs synchronous to X2X Link
		1	A/D converter does not run synchronous to X2X Link
3 - 7	Reserved	-	

A/D configuration

The sampling rate and measurement range for the A/D converter can be configured in this register.

Bit	Description	Value	Information
0 - 3	Data rate f_{DATA} (samples per second):	0000	2.5
		0001	5
		0010	10
		0011	15
		0100	25
		0101	30
		0110	50
		0111	60
		1000	100
		1001	500
		1010	1000
		1011	2000
		1100	3750
		1101	7500
		1110	Synchronous mode[1)]
		1111	Reserved
4 - 5	Standard measurement range (bit 6 = 0)	00	16 mV/V
		01	8 mV/V
		10	4 mV/V
		11	2 mV/V
	Extended measurement range (bit 6 = 1)[2)]	00	256 mV/V
		01	128 mV/V
		10	64 mV/V
		11	32 mV/V
6	Measurement range	0	Standard measurement range (2 to 16 mV/V)
		1	Extended measurement range (32 to 256 mV/V)[2)]
7	Reserved	0	(must be 0)

1) A/D converter is operated synchronously with X2X Link if possible; beginning with firmware 2
2) Starting with Firmware Version 4

7.3.6.2 X20AIx222

Register	Name	Bytes	Module							
			X20AI2222		X20AI2222-C01		X20AI4222		X20AI4222-C01	
Input:										
0	Analog input 1	2	Word		Word		Word		Word	
2	Analog input 2	2	Word		Word		Word		Word	
4	Analog input 3	2					Word		Word	
6	Analog input 4	2					Word		Word	
30	Input status[1]	1	[2]		[2]		[2]		[2]	
Output:										
16	Input filter	1		[2]		[2]		[2]		[2]
20	Lower limit value	2				[2]				[2]
22	Upper limit value	2				[2]				[2]
Data bytes in DP frame			4 in	0 out	4 in	0 out	8 in	0 out	8 in	0 out

1) Diagnostics information is automatically sent to the PROFIBUS DP master.
2) The register is transferred acyclically.

Support with firmware version ≥ V1.43

Analog input

The analog input value is mapped in this register.

Values	Input signal:
-32,768 to 32,767	Voltage signal -10 to 10 VDC

Input status

This register is used to monitor the module inputs. A change in the monitoring status generates an error message. The diagnostics function can be individually deactivated for each channel via the "Channel Diagnose x" parameter (Disable).

Bit	Description	Value	Information
0 - 1	Channel 1	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
2 - 3	Channel 2	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
4 - 5	Channel 3 (only X20AI4222)	x	Values same as channel 1
6 - 7	Channel 4 (only X20AI4222)	x	Values same as channel 1

Limiting the analog value

In addition to the status information, the analog value is set to the values listed below by default when an error occurs. The analog value is limited to the new values if the limit values were changed.

Error status	Digital value for error (default values)
Open line	+32767 (0x7FFF)
Upper limit value exceeded	+32767 (0x7FFF)
Lower limit value exceeded	-32767 (0x8001)
Invalid value	-32768 (0x8000)

Input filter

This register is used to define the filter level and input ramp limitation of the input filter, which are valid globally for all inputs.

Bit	Description	Value	Information
0 - 2	Defines the filter level	000	Filter switched off
		001	Filter level 2
		010	Filter level 4
		011	Filter level 8
		100	Filter level 16
		101	Filter level 32
		110	Filter level 64
		111	Filter level 128
3	Reserved	0	
4 - 6	Defines the input ramp limitation	000	The input value is used without limitation
		001	Limit value = 0x3FFF (16383)
		010	Limit value = 0x1FFF (8191)
		011	Limit value = 0x0FFF (4095)
		100	Limit value = 0x07FF (2047)
		101	Limit value = 0x03FF (1023)
		110	Limit value = 0x01FF (511)
		111	Limit value = 0x00FF (255)
7	Reserved	0	

Lower limit value

This register can be used to configure the lower limit for analog values. If the analog value goes below the limit value, it is frozen at this value and the corresponding error status bit is set.

Values
-32767 to 32767

Information:

The default value of -32767 corresponds to the minimum default value of -10 VDC.

Keep in mind that this setting applies to all channels!

Upper limit value

This register can be used to configure the upper limit for analog values. If the analog value goes above the limit value, it is frozen at this value and the corresponding error status bit is set.

Values
-32767 to 32767

Information:

The default value of 32767 corresponds to the maximum default value at +10 VDC.

Keep in mind that this setting applies to all channels!

7.3.6.3 X20AI2237

Register	Name	Bytes	Module			
			X20AI2237		X20AI2237-C01	
Input:						
0	Analog input 1	2	Word		Word	
2	Analog input 2	2	Word		Word	
Output:						
386	Channel configuration 1	2		1)		1)
430	Channel configuration 2	2		1)		1)
390	Configuring filters 1	2				1)
398	Lower limit value 1	2				1)
402	Upper limit value 1	2				1)
410	Lower replacement value 1	2				1)
414	Upper replacement value 1	2				1)
434	Configuring filters 2	2				1)
442	Lower limit value 2	2				1)
446	Upper limit value 2	2				1)
454	Lower replacement value 2	2				1)
458	Upper replacement value 2	2				1)
Data bytes in DP frame			4 in	0 out	4 in	0 out

1) The register can be modified in the parameter dialog box for the I/O module and is transferred acyclically.

Support with firmware version ≥ V1.43

Analog input

These registers generate the input values taking the limit value monitoring and replacement value strategy setting into account.

Values
-32767 to 32767
-10000 to 10000

Channel configuration

These registers are used to predefine the operating parameters that the module will be using for the respective channel. Each channel must be enabled individually and can be configured and operated independently.

It is extremely important to not that different limit values need to be configured for any display normalizing that needs to take place.

Bit	Name	Value	Information
0	Channel (on/off)	0	Disabled
		1	Enabled
1	Limit exceeded	0	Disabled
		1	Enabled
2	Lower limit violation	0	Disabled
		1	Enabled
3	Reserved	0	
4	Replacement value strategy	0	Replace with static value
		1	Retain last valid value
5	Measurement value scaling	0	±32767 (resolution: 16-bit)
		1	±10000 (resolution: >14-bit)
6 - 15	Reserved	0	

Configuring filters

This register is used to define the filter level and input ramp limitation of the input filter.

Bit	Description	Value	Information
0 - 2	Defines the filter level	000	Filter switched off
		001	Filter level 2
		010	Filter level 4
		011	Filter level 8
		100	Filter level 16
		101	Filter level 32
		110	Filter level 64
		111	Filter level 128
3	Reserved	0	
4 - 6	Defines the input ramp limit	000	The input value is used without limitation
		001	Limit value = 0x3FFF (16383)
		010	Limit value = 0x1FFF (8191)
		011	Limit value = 0x0FFF (4095)
		100	Limit value = 0x07FF (2047)
		101	Limit value = 0x03FF (1023)
		110	Limit value = 0x01FF (511)
		111	Limit value = 0x00FF (255)
7	Reserved	0	

Lower limit value

If the value range needs to be restricted further, this register can be used to enter new user-specific lower limit values.

Values
-32767 to 32767
-10000 to 10000

Information:

The defined limit values must take the configured scaling into consideration.

Upper limit value

If the value range needs to be restricted further, this register can be used to enter new user-specific upper limit values.

Values
-32767 to 32767
-10000 to 10000

Information:

The defined limit values must take the configured scaling into consideration.

Lower replacement value

This register is used to define the lower static values to be displayed instead of the current measured value when the limit is violated.

Values
-32767 to 32767

Upper replacement value

This register is used to define the static values to be displayed instead of the current measured value when the limit is violated.

Values
-32767 to 32767

7.3.6.4 X20AIx322

Register	Name	Bytes	Module							
			X20AI2322		X20AI2322-C01		X20AI4322		X20AI4322-C01	
Input:										
0	Analog input 1	2	Word		Word		Word		Word	
2	Analog input 2	2	Word		Word		Word		Word	
4	Analog input 3	2					Word		Word	
6	Analog input 4	2					Word		Word	
30	Input status[1)]	1	[2)]		[2)]		[2)]		[2)]	
Output:										
16	Input filter	1		[2)]		[2)]		[2)]		[2)]
18	Measurement range configuration	1		[2)]		[2)]		[2)]		[2)]
20	Lower limit value	2				[2)]				[2)]
22	Upper limit value	2				[2)]				[2)]
Data bytes in DP frame			4 in	0 out	4 in	0 out	8 in	0 out	8 in	0 out

1) Diagnostics information is automatically sent to the PROFIBUS DP master.
2) The register is transferred acyclically.

Support with firmware version ≥ V1.43

Analog input

The analog input value is mapped in this register.

Values	Information
0 to 32,767	Current signal 0 to 20 mA
-8192 to 32767	Current signal 4 to 20 mA

Input status

This register is used to monitor the module inputs. A change in the monitoring status generates an error message. The diagnostics function can be individually deactivated for each channel via the "Channel Diagnose x" parameter (Disable).

Bit	Description	Value	Information
0 - 1	Channel 1	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
2 - 3	Channel 2	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
4 - 5	Channel 3 (only X20AI4322)	x	Values same as channel 1
6 - 7	Channel 4 (only X20AI4322)	x	Values same as channel 1

Limiting the analog value

In addition to the status information, the analog value is set to the values listed below by default when an error occurs. The analog value is limited to the new values if the limit values were changed.

Error status	Digital value for error (default values)	
	0 to 20 mA	4 to 20 mA
Upper limit value exceeded	+32767 (0x7FFF)	
Lower limit value exceeded	0	-8191 (0xE001)

Input filter

This register is used to define the filter level and input ramp limitation of the input filter, which are valid globally for all inputs.

Bit	Description	Value	Information
0 - 2	Defines the filter level	000	Filter switched off
		001	Filter level 2
		010	Filter level 4
		011	Filter level 8
		100	Filter level 16
		101	Filter level 32
		110	Filter level 64
		111	Filter level 128
3	Reserved	0	
4 - 6	Defines the input ramp limitation	000	The input value is used without limitation
		001	Limit value = 0x3FFF (16383)
		010	Limit value = 0x1FFF (8191)
		011	Limit value = 0x0FFF (4095)
		100	Limit value = 0x07FF (2047)
		101	Limit value = 0x03FF (1023)
		110	Limit value = 0x01FF (511)
		111	Limit value = 0x00FF (255)
7	Reserved	0	

Measurement range configuration

The current signal range can be configured in this register. This is determined by how they are configured. The following input signals can be set:

- 0 to 20 mA current signal
- 4 to 20 mA current signal

Bit	Description	Value	Information
0 - 1	Reserved	1	
2 - 3	Reserved	0	
4	Channel 1: Current measurement range	0	0 to 20 mA current signal
		1	4 to 20 mA current signal
5	Channel 2: Current measurement range	0	0 to 20 mA current signal
		1	4 to 20 mA current signal
6 - 7	Reserved	0	

Lower limit value

This register can be used to configure the lower limit for analog values. If the analog value goes below the limit value, it is frozen at this value and the corresponding error status bit is set.

Values
-32,768 to 32,767

Information:

- **When configured as 0 to 20 mA, this value should be set to 0.**
- **When configured as 4 to 20 mA, this value can be set to -8192 (corresponds to 0 mA) in order to display values <4 mA.**

Keep in mind that this setting applies to all channels!

Upper limit value

This register can be used to configure the upper limit for analog values. If the analog value goes above the limit value, it is frozen at this value and the corresponding error status bit is set.

Values
-32,768 to 32,767

Information:

The default value of 32767 corresponds to the maximum default value at 20 mA.

Keep in mind that this setting applies to all channels!

7.3.6.5 X20AI2437

Register	Name	Bytes	Module	
			X20AI2437 X20AI2437-C01	
Input:				
0	Analog input 1	2	Word	
2	Analog input 2	2	Word	
Output:				
386	Channel configuration Channel 1	2		1)
426	Channel configuration Channel 2	1		1)
Data bytes in DP frame			4 in	0 out

1) The register is transferred acyclically.

Analog input

These registers take the values from the input registers and use them to generate the evaluated input values. The configured auxiliary functions are applied to form these values.

Values	Information
0 to 25000	Normalizing option 0 to 25 mA
0 to 32767	Normalizing option 0 to 25 mA
-8192 to 32767	Normalizing option 4 to 20 mA (value 0 corresponds to 4 mA)
0 to 65,535	Normalizing option 0 to 25 mA

Predefining values and timing

The value 0 (null) is output to the input registers until a signal short circuit or converter error causes the value to be changed.

The timing for acquiring measurement values is determined by the converter hardware and the set sampling rate. The two channels are converted independently of each other and are not synchronized with the X2X Link.

Conversion time
Channel 0x sampling rate

Channel configuration

Activates or deactivates channel 1 / 2; Sets the mode (0 - 25 mA, 4 - 20 mA, ...) for channel 1 / 2

Bit	Name	Value	Information
0	Channel	0	Channel 0x turned off
		1	Channel 0x enabled
1	Open line detection	0	Open line monitoring turned off
		1	Open line monitoring enabled
2	Underflow detection	0	Underflow detection turned off
		1	Underflow detection enabled
3	Replacement value strategy	0	Use replacement values if error occurs
		1	Keep the last valid converted value
4 - 5	Normalization	00	Displaying 0 to 25 mA as 0 to 32767
		01	Displaying 0 to 25 mA as 0 to 25000 [µA]
		10	Displaying 4 to 20 mA as 0 to 32767
		11	Displaying 0 to 25 mA as 0 to 65535
6 - 15	Reserved	-	

7.3.6.6 X20AI2438

Register	Name	Bytes	Module X20(c)AI2438	
Input:				
0	Analog input 1	2	Word	
2	Analog input 2	2	Word	
1857	Input sequence	1	Byte	
1859	RxByte 1	1	Byte	
1861	RxByte 2	1	Byte	
1863	RxByte 3	1	Byte	
1865	RxByte 4	1	Byte	
1867	RxByte 5	1	Byte	
1869	RxByte 6	1	Byte	
1871	RxByte 7	1	Byte	
Output:				
1889	Output sequence	1		Byte
1891	TxByte 1	1		Byte
1893	TxByte 2	1		Byte
1895	TxByte 3	1		Byte
1897	TxByte 4	1		Byte
1899	TxByte 5	1		Byte
1901	TxByte 6	1		Byte
1903	TxByte 7	1		Byte
Data bytes in DP frame			12 in	8 out

Support with firmware version ≥ V1.43

Analog input

These registers take the values from the input registers and use them to generate the evaluated input values. The configured auxiliary functions are applied to form these values.

Values	Information
0 to 65,535	Normalizing option 0 to 25 mA

Predefining values and timing

The value 0 (null) is output to the input registers until a signal short circuit or converter error causes the value to be changed.

The timing for acquiring measurement values is determined by the converter hardware and the set sampling rate. The two channels are converted independently of each other and are not synchronized with the X2X Link.

Conversion time
Channel 0x sampling rate

RxByte

The Tx and Rx bytes are cyclic registers used to transport the payload data and the necessary control bytes. The number of active Tx and Rx bytes is taken from the configuration of the OutputMTU and InputMTU registers, respectively.
In the user program, only the Tx and Rx bytes from the CPU can be used. The corresponding counterparts are located in the module and are not accessible to the user. For this reason, names were chosen from the CPU point of view.

- "T" - "Transmit" →CPU *transmits* data to the module.
- "R" - "Receive" →CPU *receives* data from the module.

Values
0 to 65,535

TxByte

See RxByte

Input sequence

This register contains information about the communication status of the module. It is written by the module and should only be read by the CPU.

Bit	Name	Value	Information
0 - 2	Input sequence counter	0 to 7	Counter for sequences issued in the input direction
3	InputSynchronous	0	Not ready (disabled)
		1	Ready (enabled)
4 - 6	Acknowledged output sequence	0 to 7	Mirrors the output sequence counter value
7	OutputSynchronous	0	Not ready (disabled)
		1	Ready (enabled)

Input sequence counter

The input sequence counter is a continuous counter of sequences that have been issued by the module. The module uses the input sequence counter to direct the CPU to accept a sequence (the input direction must be synchronized when this happens).

InputSynchronous

The module uses this to attempt to synchronize the input channel.

Acknowledged output sequence

This value is used for acknowledgment. The value of the output sequence counter is mirrored if the module has received a sequence successfully.

OutputSynchronous

This bit acknowledges the synchronization of the output channel for the CPU. This indicates that the module is ready to receive data.

Output sequence

This register contains information about the communication status of the CPU. It is written by the CPU and read by the module.

Bit	Name	Value	Information
0 - 2	Output sequence counter	0 to 7	Counter for sequences issued in the output direction
3	OutputSynchronous	0	Output direction disabled
		1	Output direction enabled
4 - 6	Acknowledged input sequence	0 to 7	Mirrors the input sequence counter value
7	InputSynchronous	0	Input direction not ready (disabled)
		1	Input direction ready (enabled)

Output sequence counter

The output sequence counter is a continuous counter of sequences that have been issued by the CPU. The CPU uses the output sequence counter to direct the module to accept a sequence (the output direction must be synchronized when this happens).

OutputSynchronous

The CPU uses this bit to attempt to synchronize the output channel.

Acknowledged input sequence

This value is used for acknowledgment. The value of the input sequence counter is mirrored if the CPU has received a sequence successfully.

InputSynchronous

This bit acknowledges the synchronization of the input channel for the module. This indicates that the CPU is ready to receive data.

7.3.6.6.1 X20AI2438-C0x

Register	Name	Bytes	Module			
			X20(c)AI2438-C01		X20(c)AI2438-C02	
Input:						
0	Analog input 1	2	Word		Word	
8	Analog input 2	2	Word		Word	
30	Reserved	1	Byte		Byte	
	Input status 1	1	Byte		Byte	
31	Reserved	1	Byte		Byte	
	Input status 2	1	Byte		Byte	
636	Value of the process variables 1 (HighWord) Channel 1	2	Word			
	Value of the process variables 1 (LowWord) Channel 1	2	Word			
641	Reserved	1	Byte			
	HART code 1 Channel 1	1	Byte			
660	Value of the process variables 2 (HighWord) Channel 1	2	Word			
	Value of the process variables 2 (LowWord) Channel 1	2	Word			
665	Reserved	1	Byte			
	HART code 2 Channel 1	1	Byte			
1148	Value of the process variables 1 (HighWord) Channel 2	2	Word			
	Value of the process variables 1 (LowWord) Channel 2	2	Word			
1153	Reserved	1	Byte			
	HART code 1 Channel 2	1	Byte			
1172	Value of the process variables 2 (HighWord) Channel 2	2	Word			
	Value of the process variables 2 (LowWord) Channel 2	2	Word			
1177	Reserved	1	Byte			
	HART code 2 Channel 2	1	Byte			
Data bytes in DP frame			32 in	0 out	8 in	0 out

Support with firmware version ≥ V1.43

Analog input

These registers take the values from the input registers and use them to generate the evaluated input values. The configured auxiliary functions are applied to form these values.

Values	Information
0 to 65,535	Normalizing option 0 to 25 mA

Predefining values and timing

The value 0 (null) is output to the input registers until a signal short circuit or converter error causes the value to be changed.

The timing for acquiring measurement values is determined by the converter hardware and the set sampling rate. The two channels are converted independently of each other and are not synchronized with the X2X Link.

Conversion time
Channel 0x sampling rate

Input status

The current error status of the module channels is displayed in this register, regardless of the configured replacement value strategy. Some error information may be delayed according to the previously configured condition.

Bit	Name	Value	Information
0	Underflow	0	No error
		1	Underflow on Channel 0x
1	Overrun	0	No error
		1	Overflow on Channel 0x
2	Open line	0	No error
		1	Open line on Channel 0x
3	Conversion error	0	No error
		1	Conversion error on Channel 0x
4	Composite error	0	No error
		1	Composite error on Channel 0x
5	Reserved	-	
6	Sensor error	0	No error
		1	Sensor error on Channel 0x
7	I/O supply error	0	No error
		1	I/O supply error on Channel 0x

Underflow
The signal underflow error status is indicated here according to the configuration. This error information is enabled as a multiple of the converter cycle only after the configurable delay time.

Overflow
The signal overflow error status is indicated here according to the configuration. This error information is enabled as a multiple of the converter cycle only after the configurable delay time.

Open line
According to the configuration, measurement information is checked for values <2 mA to detect a failure signal. Open line detection takes place using a configurable hysteresis value (default: 100 µA). It is possible to disable open line detection to suppress alarms when hardware is not present. This error information is enabled as a multiple of the converter cycle only after the configurable delay time.

Conversion error
This error status is triggered when the hardware exceeds the conversion time.

Composite error
This error information derives from the status of individual errors and is only activated after the configurable delay time has passed [ms]. Linking this error information to an application makes it possible to hide temporary temperature value overflows and underflows, for example.

Sensor error
This error is activated immediately after a fault is detected in the internal sensor supply.

I/O supply error
This error is activated immediately as soon as the module detects that the necessary supply voltage is no longer being provided (<20 VDC).

Value of the process variables

These registers return the current value of the process variable that has been read.

Information:

These registers are of data type REAL, which means that the available bytes on the X2X Link are filled more quickly when operated cyclically. If information from several slave nodes is needed, it must be retrieved acyclically or using FlatStream.

Data type	Values	Information
REAL	IEEE745 SPF	32-bit data type with valid value
	0x7FA00000	Not a number (NaN) with invalid value

HART code

These registers return a HART-specific code that specifies the unit for the measured value. The coding for this is established in the HART specification.

Values
See description of the HART slave See HART specification

7.3.6.7 X20AIx622

Register	Name	Bytes	Module							
			X20AI2622		X20AI2622-C01*		X20(c)AI4622		X20(c)AI4622-C01*	
Input:										
0	Analog input 1	2	Word		Word		Word		Word	
2	Analog input 2	2	Word		Word		Word		Word	
4	Analog input 3	2					Word		Word	
6	Analog input 4	2					Word		Word	
30	Input status[1)]	1	[2)]		[2)]		[2)]		[2)]	
Output:										
16	Input filter	1		[2)]		[2)]		[2)]		[2)]
18	Measurement range configuration	1		[2)]		[2)]		[2)]		[2)]
20	Lower limit value	2				[2)]				[2)]
22	Upper limit value	2				[2)]				[2)]
Data bytes in DP frame			4 in	0 out	4 in	0 out	8 in	0 out	8 in	0 out

1) Diagnostics information is automatically sent to the PROFIBUS DP master.
2) The register is transferred acyclically.

Module names with '*': Support with firmware version ≥ V1.43

Analog input

The analog input value is mapped in this register depending on the configured operating mode.

Values	Input signal:
-32,768 to 32,767	Voltage signal -10 to 10 VDC
0 to 32,767	Current signal 0 to 20 mA

Input status

This register is used to monitor the module inputs. The diagnostics function can be individually deactivated for each channel via the "Channel Diagnose x" parameter (Disable). A change in the monitoring status generates an error message. The following states are monitored depending on the settings:

Value	Voltage signal ±10 V	Current signal 0 to 20 mA	Current signal 4 to 20 mA
0	No error	No error	No error
1	Lower limit value exceeded	Default setting The input value has a lower limit of 0x0000. Underflow monitoring is therefore not necessary. After lower limit value change The input value is limited to the configured value. The status bit is set when the lower limit value is passed.	Lower limit value exceeded
2	Upper limit value exceeded	Upper limit value exceeded	Upper limit value exceeded
3	Open line	-	-

Bit	Description	Value	Information
0 - 1	Channel 1	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
2 - 3	Channel 2	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
4 - 5	Channel 3 (only X20AI4622)	x	Values same as channel 1
6 - 7	Channel 4 (only X20AI4622)	x	Values same as channel 1

Limiting the analog value

In addition to the status information, the analog value is fixed to the values listed below by default in an error state. The analog value is limited to the new values if the limit values were changed.

Error state	Digital value on error (default values)
Open circuit	+32767 (0x7FFF)
Upper limit value overshot	+32767 (0x7FFF)
Lower limit value undershot	-32767 (0x8001)
Invalid value	-32768 (0x8000)

Input filter

This register is used to define the filter level and input ramp limitation of the input filter, which are valid globally for all inputs.

Bit	Description	Value	Information
0 - 2	Defines the filter level	000	Filter switched off
		001	Filter level 2
		010	Filter level 4
		011	Filter level 8
		100	Filter level 16
		101	Filter level 32
		110	Filter level 64
		111	Filter level 128
3	Reserved	0	
4 - 6	Defines the input ramp limitation	000	The input value is used without limitation
		001	Limit value = 0x3FFF (16383)
		010	Limit value = 0x1FFF (8191)
		011	Limit value = 0x0FFF (4095)
		100	Limit value = 0x07FF (2047)
		101	Limit value = 0x03FF (1023)
		110	Limit value = 0x01FF (511)
		111	Limit value = 0x00FF (255)
7	Reserved	0	

Measurement range configuration

This register can be used to define the type and range of signal measurement.

Each channel is capable of handling either current or voltage signals. This differentiation is made using multiple connection terminal points and an integrated switch in the module. The switch is automatically activated by the module depending on the specified configuration. The following input signals can be set:

- ±10 V voltage signal (default)
- 0 to 20 mA current signal
- 4 to 20 mA current signal

Bit	Description	Value	Information
0	Channel 1	0	Voltage signal
		1	Current signal, measurement range corresponding to bit 4
1	Channel 2	0	Voltage signal
		1	Current signal, measurement range corresponding to bit 7
2	Channel 3 (only X20AI4622)	x	Values same as channel 1
3	Channel 4 (only X20AI4622)	x	Values same as channel 1
4	Channel 1: Current measurement range	0	0 to 20 mA current signal
		1	4 to 20 mA current signal
5	Channel 2: Current measurement range	0	0 to 20 mA current signal
		1	4 to 20 mA current signal
6	Channel 3: Current measurement range (only X20AI4622)	x	Values same as channel 1
7	Channel 4: Current measurement range (only X20AI4622)	x	Values same as channel 1

Lower limit value

This register can be used to configure the lower limit for analog values. If the analog value goes below the limit value, it is frozen at this value and the corresponding error status bit is set.

Values
-32,768 to 32,767

Information:

- **The default value of -32768 corresponds to the minimum default value of -10 VDC.**
- **When configured as 0 to 20 mA, this value should be set to 0.**
- **When configured as 4 to 20 mA, this value can be set to -8192 (corresponds to 0 mA) in order to display values <4 mA.**

Information:

Keep in mind that this setting applies to all channels!

Upper limit value

This register can be used to configure the upper limit for analog values. If the analog value goes above the limit value, it is frozen at this value and the corresponding error status bit is set.

Values
-32,768 to 32,767

Information:

The default value of 32767 corresponds to the maximum default value of 20 mA or +10 VDC.

Information:

Keep in mind that this setting applies to all channels!

7.3.6.8 X20AIx632

Register	Name	Bytes	Module							
			X20AI2632 X20AI2632-1		X20AI2632-C11		X20AI2632-C12		X20AI2632-C13	
Input:										
0	Analog input 1	2	Word		Word		Word		Word	
4	Analog input 2	2	Word		Word		Word		Word	
641	**HI:** 0 **LO:** Status of the channels	2							Word	
Output:										
257	Input configuration 1	1		1)		1)		1)		1)
289	Input configuration 2	1		1)		1)		1)		1)
276	Gain 1	1				2)		2)		2)
308	Gain 2	1				2)		2)		2)
284	Offset 1	1				2)		2)		2)
316	Offset 2	1				2)		2)		2)
259	Filter order 1	1						1)		1)
291	Filter order 2	1						1)		1)
262	Cutoff frequency 1	2						1)		1)
294	Cutoff frequency 2	2						1)		1)
Data bytes in DP frame			4 in	0 out	4 in	0 out	4 in	0 out	6 in	0 out

1) The register can be modified in the parameter dialog box for the I/O module and is transferred acyclically.
2) The register is transferred acyclically.

Register	Name	Bytes	Module							
			X20AI4632 X20AI4632-1		X20AI4632-C11		X20AI4632-C12		X20AI4632-C13	
Input:										
0	Analog input 1	2	Word		Word		Word		Word	
4	Analog input 2	2	Word		Word		Word		Word	
8	Analog input 3	2	Word		Word		Word		Word	
12	Analog input 4	2	Word		Word		Word		Word	
641	**HI:** 0 **LO:** Status of the channels	2							Word	
Output:										
257	Input configuration 1	1		1)		1)		1)		1)
289	Input configuration 2	1		1)		1)		1)		1)
321	Input configuration 3	1		1)		1)		1)		1)
353	Input configuration 4	1		1)		1)		1)		1)
276	Gain 1	1				2)		2)		2)
308	Gain 2	1				2)		2)		2)
340	Gain 3	1				2)		2)		2)
372	Gain 4	1				2)		2)		2)
284	Offset 1	1				2)		2)		2)
316	Offset 2	1				2)		2)		2)
348	Offset 3	1				2)		2)		2)
380	Offset 4	1				2)		2)		2)
259	Filter order 1	1						1)		1)
291	Filter order 2	1						1)		1)
323	Filter order 3	1						1)		1)
355	Filter order 4	1						1)		1)
262	Cutoff frequency 1	2						1)		1)
294	Cutoff frequency 2	2						1)		1)
326	Cutoff frequency 3	2						1)		1)
358	Cutoff frequency 4	2						1)		1)
Data bytes in DP frame			8 in	0 out	8 in	0 out	8 in	0 out	10 in	0 out

1) The register can be modified in the parameter dialog box for the I/O module and is transferred acyclically.
2) The register is transferred acyclically.

Analog input

This register contains the analog input value depending on the configured operating mode.

Values	Input signal:
-32768 to 32767	Voltage signal
0 to 32767	Current signal

Status of the channels

This register collects error messages synchronously with the network cycle. Temporary error states that were registered in a conversion cycle remain active for at least 2 network cycles. In order to receive detailed error information, the corresponding error counters and X2X network events should also be observed.

Bit	Description	Value	Information
0	Channel 1	0	OK
		1	Error
1	Channel 2	0	OK
		1	Error
2	Channel 3 (X20AI4632 only)	x	Values same as channel 1
3	Channel 3 (X20AI4632 only)	x	Values same as channel 1
4 - 5	Reserved	-	
6	SyncStatus	0	"Synchronization between X2X and conversion cycle" status OK
		1	Not synchronized
7	ConversionCycle	0	OK
		1	Error

Input configuration

These registers are used to configure the individual inputs.

The individual channels are designed for current and voltage signals. The differentiation is made by different terminal blocks; because of different adjustment values for current and voltage, the input signal must also be selected. The following input signals can be set:

- X20AIx632: ±10 V voltage signal (default)
- X20AIx632-1: ±11 V voltage signal (default)
- X20AIx632: 0 to 20 mA current signal
- X20AIx632-1: 0 to 22 mA current signal

Filtering, analysis and error monitoring (bits 4 to 6) can only be used if the channel is enabled (bit 7 = 0).

Bit	Description	Value	Information
0	Terminal selector	0	Voltage terminal
		1	Current terminal
1	Gain selector	0	Voltage
		1	Current
2 - 3	Reserved	-	
4	Filtering active	0	Inactive
		1	Active
5	Minimum/Maximum analysis active	0	Inactive
		1	Active
6	Error monitoring active	0	Inactive
		1	Active
7	Enables channel	0	Channel enabled
		1	Channel disabled

Gain

The user-defined gain for the A/D converter data of the respective physical channels can be specified in these registers.

The value 65,536 (0x10000) corresponds to a gain of 1.

Values
-2,147,483,648 to 2,147,483,647

The raw and filtered A/D converter data is compared and normalized (gain = k, offset = d). In addition, user-defined normalization is available using the following registers:

- Gain (ku)
- Offset (du)

The execution time is optimized by grouping the factors together.

System scaling calculation:

nom = k * RawValue + d

k = k * ku

d = k * d + du

The value must be limited since it can exceed the 16-bit constraints.

Offset

The user-defined offset for the A/D converter data can be specified in this register. See also Gain

The value 65,536 (0x10000) corresponds to an offset of 1.

Values
-2,147,483,648 to 2,147,483,647

Filter order

The filter order is specified in this register. Register Cutoff frequency is used for configuration of the respective cutoff frequency of the low-pass filter.

Values
1 to 4

Internal filter orders greater than 1 are implemented as cascaded first-order filters. Since the filter is calculated in the sampling cycle, the filter characteristics are directly related to the settings for the sampling cycle time.

Calculations for effective cascading limit frequency for the N-order filter:

$$fc1 = \frac{fcN}{(2^{\frac{1}{N}} - 1)^{\frac{1}{2}}}$$

Approximate calculation of filter cascade with sample time "Ts":

yn = a * xn + b * y(n-1)

a = Ts / (Ts + 1/fc)

b = 1 - a

Information:

Errors related to the sample time and filter order can occur as a result of the method used to calculate the low-pass filter.

Cutoff frequency

The cutoff frequency of the respective low-pass filter is configured in these registers.

The highest cutoff frequency is limited by the Nyquist Shannon sampling theory (based on the sampling cycle time). The system does not check for violations of this sampling theorem.

Values	Description
1 to 65535	Cutoff frequency in hertz

7.3.6.9 X20AI8221

Register	Name	Bytes	Module			
			X20AI8221		X20AI8221-C01	
Input:						
0	Analog input 1	2	Word		Word	
2	Analog input 2	2	Word		Word	
4	Analog input 3	2	Word		Word	
6	Analog input 4	2	Word		Word	
8	Analog input 5	2	Word		Word	
10	Analog input 6	2	Word		Word	
12	Analog input 7	2	Word		Word	
14	Analog input 8	2	Word		Word	
30	**HI:** 0 **LO:** Input status Channel 1 - 4	2			Word	
31	**HI:** 0 **LO:** Input status Channel 5 - 8	2			Word	
Output:						
16	Input filter	1		1)		1)
20	Lower limit value	2				1)
22	Upper limit value	2				1)
Data bytes in DP frame			16 in	0 out	20 in	0 out

1) The register is transferred acyclically.

Support with firmware version ≥ V1.43

Analog input

The analog input value is mapped in this register.

Values	Input signal:
-32,768 to 32,767	Voltage signal -10 to 10 VDC

Input status

This register is used to monitor the module inputs. A change in the monitoring status generates an error message.

Bit	Description	Value	Information
0 - 1	Channel 1 or 5	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
...		...	
6 - 7	Channel 4 or 8	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line

Limiting the analog value

In addition to the status information, the analog value is fixed to the values listed below by default in an error state. The analog value is limited to the new values if the limit values were changed.

Error state	Digital value on error (default values)
Open circuit	+32767 (0x7FFF)
Upper limit value overshot	+32767 (0x7FFF)
Lower limit value undershot	-32767 (0x8001)
Invalid value	-32768 (0x8000)

Input filter

This register is used to define the filter level and input ramp limitation of the input filter.

Bit	Description	Value	Information
0 - 2	Defines the filter level	000	Filter switched off
		001	Filter level 2
		010	Filter level 4
		011	Filter level 8
		100	Filter level 16
		101	Filter level 32
		110	Filter level 64
		111	Filter level 128
3	Reserved	0	
4 - 6	Defines the input ramp limitation	000	The input value is used without limitation
		001	Limit value = 0x3FFF (16383)
		010	Limit value = 0x1FFF (8191)
		011	Limit value = 0x0FFF (4095)
		100	Limit value = 0x07FF (2047)
		101	Limit value = 0x03FF (1023)
		110	Limit value = 0x01FF (511)
		111	Limit value = 0x00FF (255)
7 - 15	Reserved	0	

Lower limit value

This register can be used to configure the lower limit for analog values. If the analog value goes below the limit value, it is frozen at this value and the corresponding error status bit is set.

Values
-32,768 to 32,767

Information:

The default value of -32768 corresponds to the minimum default value of -10 VDC.

Keep in mind that this setting applies to all channels!

Upper limit value

This register can be used to configure the upper limit for analog values. If the analog value goes above the limit value, it is frozen at this value and the corresponding error status bit is set.

Values
-32,768 to 32,767

Information:

The default value of 32767 corresponds to the maximum default value at +10 VDC.

Keep in mind that this setting applies to all channels!

7.3.6.10 X20AI8321

Register	Name	Bytes	Module			
			X20AI8321		X20AI8321-C01	
Input:						
0	Analog input 1	2	Word		Word	
2	Analog input 2	2	Word		Word	
4	Analog input 3	2	Word		Word	
6	Analog input 4	2	Word		Word	
8	Analog input 5	2	Word		Word	
10	Analog input 6	2	Word		Word	
12	Analog input 7	2	Word		Word	
14	Analog input 8	2	Word		Word	
30	**HI:** 0 **LO:** Input status Channel 1 - 4	2			Word	
31	**HI:** 0 **LO:** Input status Channel 5 - 8	2			Word	
Output:						
16	Input filter	1		1)		1)
18	Measurement range configuration	1		1)		1)
20	Lower limit value	2				1)
22	Upper limit value	2				1)
Data bytes in DP frame			16 in	0 out	20 in	0 out

1) The register is transferred acyclically.

Support with firmware version ≥ V1.43

Analog input

The analog input value is mapped in this register.

Values	Input signal:
0 to 32,767	Current signal 0 to 20 mA or 4 to 20 mA

Input status

This register is used to monitor the module inputs. A change in the monitoring status generates an error message.

Bit	Description	Value	Information
0 - 1	Channel 1 or 5	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
...		...	
6 - 7	Channel 4 or 8	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded

Limiting the analog value

In addition to the status information, the analog value is set to the values listed below by default when an error occurs. The analog value is limited to the new values if the limit values were changed.

Error status	Digital value for error (default values)	
	0 to 20 mA	4 to 20 mA
Upper limit value exceeded	+32767 (0x7FFF)	
Lower limit value exceeded	0	-8191 (0xE001)

Input filter

This register is used to define the filter level and input ramp limitation of the input filter.

Bit	Description	Value	Information
0 - 2	Defines the filter level	000	Filter switched off
		001	Filter level 2
		010	Filter level 4
		011	Filter level 8
		100	Filter level 16
		101	Filter level 32
		110	Filter level 64
		111	Filter level 128
3	Reserved	0	
4 - 6	Defines the input ramp limitation	000	The input value is used without limitation
		001	Limit value = 0x3FFF (16383)
		010	Limit value = 0x1FFF (8191)
		011	Limit value = 0x0FFF (4095)
		100	Limit value = 0x07FF (2047)
		101	Limit value = 0x03FF (1023)
		110	Limit value = 0x01FF (511)
		111	Limit value = 0x00FF (255)
7 - 15	Reserved	0	

Measurement range configuration

The current signal range can be configured in this register. This is determined by how they are configured. The following input signals can be set:

- 0 to 20 mA current signal
- 4 to 20 mA current signal

Bit	Description	Value	Information
0	Channel 1: Current measurement range	0	0 to 20 mA current signal
		1	4 to 20 mA current signal
...		...	
7	Channel 8: Current measurement range	0	0 to 20 mA current signal
		1	4 to 20 mA current signal

Lower limit value

This register can be used to configure the lower limit for analog values. If the analog value goes below the limit value, it is frozen at this value and the corresponding error status bit is set.

Values
-32,768 to 32,767

Information:

- **When configured as 0 to 20 mA, this value should be set to 0.**
- **When configured as 4 to 20 mA, this value can be set to -8192 (corresponds to 0 mA) in order to display values <4 mA.**

Keep in mind that this setting applies to all channels!

Upper limit value

This register can be used to configure the upper limit for analog values. If the analog value goes above the limit value, it is frozen at this value and the corresponding error status bit is set.

Values
-32,768 to 32,767

Information:

The default value of 32767 corresponds to the maximum default value at 20 mA.

Keep in mind that this setting applies to all channels!

7.3.6.11 X20AIx744

Register	Name	Bytes	Module			
			X20AIA744		X20AIB744	
Input:						
4	Analog input 1	4	Long		Long	
12	Analog input 2	4	Long		Long	
20	Analog input 3	4			Long	
28	Analog input 4	4			Long	
33	**HI:** Reserved **LO:**Status packed 1	2	Word		Word	
35	**HI:** Reserved **LO:**Status packed 2	2	Word		Word	
37	**HI:** Reserved **LO:**Status packed 3	2			Word	
39	**HI:** Reserved **LO:**Status packed 4	2			Word	
Output:						
2	Control packed 1	2		Word		Word
6	Control packed 2	2		Word		Word
10	Control packed 3	2				Word
14	Control packed 4	2				Word
Data bytes in DP frame			12 in	4 out	24 in	8 out

Analog input

This register contains the analog input value.

Values	Input signal:
≤-8,388,608	Negative invalid range
-8,388,607	Negative full-scale deflection / Underflow
-8,388,606 to 8388606	Valid range
8,388,607	Positive full-scale deflection / Overflow / Open circuit
≥8,388,608	Positive invalid range

Status packed

These registers contain the state of the analog inputs.

Bit	Description	Value	Information
0	I/O power supply	0	No error
		1	Error in power supply
1	Bypass current	0	No error
		1	Overcurrent (sum from all sensors)
2 - 3	Reserved	0	
4	A/D converter configuration	0	Already configured
		1	Not yet configured
5	Analog values	0	Analog value valid
		1	Analog value invalid (analog value = 0xFF800000). Possible causes: • Internal transfer error (XOR checksum verification) • Error in strain gauge supply (bit 1) • Error in I/O power supply (bit 0) • A/D converter not (yet) configured
6	Analog value range overflow	0	Analog value valid
		1	Analog value invalid. Possible causes: • Overflow / Open circuit (analog value = 0x007FFFFF) • Underflow (analog value = 0xFF800001)
7	Moving average filter	0	Moving average filter tuned
		1	Moving average filter not tuned. Possible causes: • After changing the filter length • Consequence of the filter being reset by another error

Control packed

The strain gauge inputs are configured in these registers:

- Strain gauge factor of strain gauge load cell
- Enabling of filters

Bit	Description	Value	Information	
0 - 2	Strain gauge factor	000	Default: 256 mV/V	
		001	128 mV/V	
		010	64 mV/V	
		011	32 mV/V	
		100	16 mV/V	
		101	8 mV/V	
		110	4 mV/V	
		111	2 mV/V	
			Averaging	1. Notch frequency [Hz]
3 - 7	Moving average	00000	Default: Moving average disabled (bypass)	
		00001	2	2500
		00010	4	1250
		00011	5	1000
		00100	10	500
		00101	20	250
		00110	25	200
		00111	50	100
		01000	83	60
		01001	100	50
		01010	125	40
		01011	167	30
		01100	200	25
		01101	250	20
		01110	300	16.66
		01111	500	10
		10000	1000	5
		10001 to 11111	Reserved (firmware limited to 1000)	
8	Notch filter	0	Default: IIR notch filter disabled (bypass)	
		1	IIR notch filter enabled	
9	Reserved	0		
10 - 11	Low-pass filter mode	00	IIR low-pass filter disabled (bypass)	
		01	First-order IIR low-pass filter (see IIR low-pass filter)	
		10 - 11	Reserved: No IIR low-pass filter active	
			Filter level	-3 db frequency [Hz]
12 - 14	Low-pass filter level	000	1	575
		001	2	230
		010	3	106
		011	4	51
		100	5	25
		101	6	12.5
		110	7	6.2
		111	8	3.1
15	Reserved	0		

Filter

An independent cascade of filters is available for each channel. They can be individually enabled and configured at runtime. By default, all filters are disabled when the device is switched on. The filters are controlled and configured using register Control packed.

In order to allow the filter behavior to be adapted to the measuring situation or machine cycle (high dynamics and low precision or low dynamics and high precision), the filter characteristics of both the IIR low-pass filter as well as the moving average filter can be changed synchronously at any time.

IIR low-pass filter

The IIR low-pass filter is used to generally smooth and increase the resolution of the analog value. The filter works according to the following formula:

$$y = y_{Old} + \frac{x - y_{Old}}{2^{Filter\ level}}$$

x ... Current filter input value
y_{Old} ... Old filter output value
y ... New filter output value

Parameter "Filter level" in the formula above is set using register Control packed. "Filter level" = 0 if the IIR low-pass filter is disabled.

Filter characteristics of the first-order IIR low-pass filter

The following table provides an overview of the -3 dB limit frequency f_c depending on the configured filter level.

IIR low-pass filter level	f_c [Hz]
1	575
2	230
3	106
4	51
5	25
6	12.5
7	6.2
8	3.1

Sinc1 / Moving average filter

Like the low-pass filter, the moving average filter can also be used to smooth out the signal and increase its resolution. In addition, configuring the filter length accordingly makes it possible to target and efficiently filter out individual interference frequencies. The source of these interference frequencies may be mechanical or electromagnetic. Multiples of these are also filtered out (as long as they are a whole-number factor of the data output rate of 5000 samples per second and channel).

Example:
Data output rate = 5000 samples/s/channel, averaging over 4 values → "Notch" at 1.25 kHz (and 2.5 kHz)

When reconfiguring the filter length from "n" to "m", it takes |m-n| * 200 µs until the desired filter length setpoint is reached again. As long as the filter length setpoint is not reached, this situation will be indicated by status bit 7 in register Status packed.

Filter characteristics of the moving average filter

Filter configuration	Filter length	f_{Notch} [Hz] 1)	f_c [Hz] 2)
0	1		
1	2	2500	1244
2	4	1250	568
3	5	1000	450
4	10	500	222
5	20	250	111
6	25	200	88.4
7	50	100	44.0
8	83	60.24	26.5
9	100	50	21.9
10	125	40	17.5
11	167	29.94	13.0
12	200	25	10.9
13	250	20	8.6
14	300	16.67	7.1
15	500	10	4.3
16	1000	5	2.0

1) Mid-band frequency of the first attenuation maximum.
2) -3 dB limit frequency.

50/60 Hz IIR notch filter

The IIR notch filter is used for narrow-band suppression of interference caused by the mains frequency.

This is an eight-order IIR notch filter implemented in the form of a cascade of 4 second-order IIR notch filters.

Information:

The IIR notch filter should only be enabled if there is actually interference being caused by the mains frequency. It is always important to check whether sufficiently low and sufficiently narrow band filtering at 50 Hz / 60 Hz can be implemented using a moving average filter (see Filter characteristics of the moving average filter).

This is because, like every higher-order IIR notch filter, this filter also has a tendency to respond to an input step with an attenuating vibration. The higher the dynamics of the expected measurement signal, the greater the potential interfering effect of this vibration tendency. In extreme cases, the vibration can temporarily be greater than the mains interference that is supposed to be filtered out.

Filter characteristics of the IIR notch filter

There are 3 different filter characteristics that can be selected for both 50 Hz and 60 Hz (-40 dB, -60 dB and -80 dB). The higher the attenuation, the narrower the stopband.

7.3.6.12 X20AP31x1

Register	Name	Bytes	Module X20AP31x1	
Input:				
130	Input status	2	Word	
266	System status 0	2	Word	
270	System status 1	2	Word	
2	PmeanT	2	Word	
4	QmeanT	2	Word	
6	SmeanT	2	Word	
8	AEnergyT	4	Long	
12	REnergyT	4	Long	
104	DPS sequence input: In 2	4	Long	
100	DPS sequence input: In 1	4	Long	
Output:				
194	Control signal evaluation	2		Word
118	DPS sequence output: Out 2	4		Long
114	DPS sequence output: Out 1	4		Long
	Data bytes in DP frame		28 in	10 out

Support with firmware version ≥ V1.43

Input status

The signals are recorded in 200 µs intervals.

Bit	Name	Value	Information
0	Energy pulse 1, total active energy	0	Not yet calculated
		1	Calculated
1	Energy pulse 2, total apparent energy, configurable Default: Arithmetic sum of apparent energy	0	Not yet calculated
		1	Calculated
2	Energy pulse 3, total active energy, fundamental wave	0	Not yet calculated
		1	Calculated
3	Energy pulse 4, total active energy, harmonics	0	Not yet calculated
		1	Calculated
4	Zero cross signal – Phase A	0	Zero cross-over not detected
		1	Default: Pulse at rising edge of the zero cross signal on the voltage input
5	Zero cross signal – Phase B	0	Zero cross-over not detected
		1	Default: Pulse at rising edge of the zero cross signal on the voltage input
6	Zero cross signal – Phase C	0	Zero cross-over not detected
		1	Default: Pulse at rising edge of the zero cross signal on the voltage input
7	Reserved	0	
8	DFT response sent	x	If the state in register Control signal evaluation corresponds to the response, then the action is complete.
9	Energy value update response sent	0	No update
		1	Update complete
10	Energy value response deleted	x	If the state in register Control signal evaluation corresponds to the response, then the action is complete.
11	Energy value response set	x	If the state in register Control signal evaluation corresponds to the response, then the action is complete.
12 - 15	Reserved	0	

System status 0

The register is read by the converter in a ~5 ms interval.

Bit	Name	Value	Information
0 - 1	Reserved	0	
2	Voltage of one or more phases < failure threshold in the register	0	Voltage within permitted range
		1	Voltage lower than the failure threshold
3	Voltage of one or more phases < warning threshold in the register	0	Voltage within permitted range
		1	Voltage lower than the warning threshold
4 - 5	Reserved	0	
6	Error in the order of phase currents	0	No error
		1	Errors
7	Error in the order of phase voltages	0	No error
		1	Errors
8	Checksum error in configuration block 3	0	No error
		1	Errors
9	Reserved	0	
10	Checksum error in configuration block 2	0	No error
		1	Errors
11	Reserved	0	
12	Checksum error in configuration block 1	0	No error
		1	Errors
13	Reserved	0	
14	Checksum error in configuration block 0	0	No error
		1	Errors
15	Reserved	0	

System status 1

Bit	Name	Value	Information
0	The direction of the active energy for phase C has changed	0	No change of direction
		1	Direction has changed
1	The direction of the active energy for phase B has changed	0	No change of direction
		1	Direction has changed
2	The direction of the active energy for phase A has changed	0	No change of direction
		1	Direction has changed
3	The direction of the active energy for the total has changed	0	No change of direction
		1	Direction has changed
4	The direction of the reactive energy for phase C has changed	0	No change of direction
		1	Direction has changed
5	The direction of the reactive energy for phase B has changed	0	No change of direction
		1	Direction has changed
6	The direction of the reactive energy for phase A has changed	0	No change of direction
		1	Direction has changed
7	The direction of the reactive energy for the total has changed	0	No change of direction
		1	Direction has changed
8	Reserved	0	
9	DFT analysis complete (temporary bit)	0	DFT analysis not complete
		1	DFT analysis complete
10	The THDIx value of one or more phases > warning threshold in the register	0	THDIx value within permitted range
		1	THDIx value higher than warning threshold
11	The THDUx value of one or more phases > warning threshold in the register	0	THDUx value within permitted range
		1	THDUx value higher than warning threshold
12 - 13	Reserved	0	
14	The calculated value of the neutral line > warning threshold in the register	0	Calculated value within permitted range
		1	Calculated value higher than warning threshold
15	The measured value of the neutral line > warning threshold in the register	0	Measured value within permitted range
		1	Measured value higher than warning threshold

PmeanT

The value in the register equals a fourth of the actual power.

Values	Information
-32767 to 32767	Resolution 4 W

This value must be multiplied by 4 by the application. Calculation formula for actual power:

Actual total active power = Register value * 4

QmeanT

The value in the register equals a fourth of the actual power.

Values	Information
-32767 to 32767	Resolution 4 var

This value must be multiplied by 4 by the application. Calculation formula for actual power:

Actual total reactive power = Register value * 4

SmeanT

The value in the register equals a fourth of the actual power. The power is calculated in arithmetic mode.

Values	Information
0 to 32,767	Resolution 4 VA

This value must be multiplied by 4 by the application. Calculation formula for actual power:

Actual total apparent power = Register value * 4

AEnergyT

Total active energy regenerated by the consumer is subtracted. The data is transferred in 2 words.

Values	
-2,147,483,647 to 2,147,483,647	Resolution 0.1 or 0.01 CF, depending on the Power Line factor (e.g. kWs)

Internal calculation formula for the total active energy:

AEnergyT = (DINT)(APenergyT - ANenergyT) ... Calculation overflows are ignored.

REnergyT

Total reactive energy regenerated by the consumer is subtracted. The data is transferred in 2 words.

Values	Information
-2,147,483,647 to 2,147,483,647	Resolution 0.1 or 0.01 CF, depending on the Power Line factor (e.g. kWs)

Internal calculation formula for the total reactive energy:

REnergyT = (DINT)(RPenergyT - RNenergyT) ... Calculation overflows are ignored.

DPS sequence input

In 1: DPS data 3 to 1 and DPS sequence byte for the flat stream register. Data is transferred in 2 words with the byte order: Data 3 to Data 1 + sequence byte.

In 2: DPS data 7 to 4 for the flat stream register. Data is transferred in 2 words with the byte order high-low.

Control signal evaluation

Control signals are evaluated in a ~5 ms interval.

Bit	Name	Value	Information
0	DFT analysis	0	Don't start
		1	Start[1)]
1	Automatically read energy values	0	Do not automatically read
		1	Automatically read
2	Clear energy values	0	Don't delete
		1	Clear[1)]
3	Set energy values	0	Don't start
		1	Start[1)]
4 - 15	Reserved	0	

1) If the state in the Control signal evaluation register corresponds with the response, then the action is complete.

DPS sequence output

Out 1: DPS data 3 to 1 and DPS sequence byte for the flat stream register. Data is transferred in 2 words with the byte order: Data 3 to Data 1 + sequence byte.

Out 2: DPS data 7 to 4 for the flat stream register. Data is transferred in 2 words with the byte order: Data 7 to Data 4.

7.3.7 Analog output modules

7.3.7.1 X20AO2437

Register	Name	Bytes	Module X20AO2437	
Input:				
30	**HI:** 0 **LO:** Status of the output 1	2	Word	
31	**HI:** 0 **LO:** Status of the output 2	2	Word	
Output:				
0	Analog output 1	2		Word
2	Analog output 2	2		Word
Data bytes in DP frame			4 in	4 out

Status of the output

The status register gives the user feedback about whether the respective channel is functioning properly.

Bit	Name	Value	Information
0 - 1	Reserved	-	
2	Wiring	0	Line OK
		1	Open line
3	Conversion temperature	0	Conversion temperature OK
		1	Conversion temperature too high
4 - 6	Reserved	-	
7	Module supply	0	Module supply OK
		1	Module supply error

Analog output

These registers provide the standardized output values. Depending on the scaling selected, the value range and the data type can be adapted to the requirements of the application. Once a permitted value is determined, the module outputs the respective current.

> **Information:**
>
> **The value "0" disables the channel status LED.**

Values
0 to 65,535

7.3.7.2 X20AO2438

Register	Name	Bytes	Module X20AO2438	
Input:				
1857	Input sequence	1	Byte	
1859	RxByte 1	1	Byte	
1861	RxByte 2	1	Byte	
1863	RxByte 3	1	Byte	
1865	RxByte 4	1	Byte	
1867	RxByte 5	1	Byte	
1869	RxByte 6	1	Byte	
1871	RxByte 7	1	Byte	
Output:				
0	Analog output 1	2		Word
2	Analog output 2	2		Word
1889	Output sequence	1		Byte
1891	TxByte 1	1		Byte
1893	TxByte 2	1		Byte
1895	TxByte 3	1		Byte
1897	TxByte 4	1		Byte
1899	TxByte 5	1		Byte
1901	TxByte 6	1		Byte
1903	TxByte 7	1		Byte
Data bytes in DP frame			8 in	12 out

Support with firmware version ≥ V1.43

Input sequence

This register contains information about the communication status of the module. It is written by the module and should only be read by the CPU.

Bit	Name	Value	Information
0 - 2	Input sequence counter	0 to 7	Counter for sequences issued in the input direction
3	InputSynchronous	0	Not ready (disabled)
		1	Ready (enabled)
4 - 6	Acknowledged output sequence	0 to 7	Mirrors the output sequence counter value
7	OutputSynchronous	0	Not ready (disabled)
		1	Ready (enabled)

Input sequence counter

The input sequence counter is a continuous counter of sequences that have been issued by the module. The module uses the input sequence counter to direct the CPU to accept a sequence (the input direction must be synchronized when this happens).

InputSynchronous

The module uses this to attempt to synchronize the input channel.

Acknowledged output sequence

This value is used for acknowledgment. The value of the output sequence counter is mirrored if the module has received a sequence successfully.

OutputSynchronous

This bit acknowledges the synchronization of the output channel for the CPU. This indicates that the module is ready to receive data.

1. The module only forms segments that are at least one byte smaller than the enabled MTU. Each sequence begins with a control byte so that the data stream is clearly structured and relatively easy to evaluate.
2. Since a FlatStream message can be of any length, the last segment of the message frequently doesn't fill up all of the MTU's space. By default, the remaining bytes during this type of transfer cycle are not used.

RxByte

The Tx and Rx bytes are cyclic registers used to transport the payload data and the necessary control bytes.
In the user program, only the Tx and Rx bytes from the CPU can be used. The corresponding counterparts are located in the module and are not accessible to the user. For this reason, names were chosen from the CPU point of view.

- "T" - "Transmit" →CPU *transmits* data to the module.
- "R" - "Receive" →CPU *receives* data from the module.

Values
0 to 65,535

Analog output

These registers provide the standardized output values. Depending on the scaling selected, the value range and the data type can be adapted to the requirements of the application. Once a permitted value is determined, the module outputs the respective current.

Information:

The value "0" disables the channel status LED.

Values
0 to 65,535

Output sequence

This register contains information about the communication status of the CPU. It is written by the CPU and read by the module.

Bit	Name	Value	Information
0 - 2	Output sequence counter	0 to 7	Counter for sequences issued in the output direction
3	OutputSynchronous	0	Output direction disabled
		1	Output direction enabled
4 - 6	Acknowledged input sequence	0 to 7	Mirrors the input sequence counter value
7	InputSynchronous	0	Input direction not ready (disabled)
		1	Input direction ready (enabled)

Output sequence counter

The output sequence counter is a continuous counter of sequences that have been issued by the CPU. The CPU uses the output sequence counter to direct the module to accept a sequence (the output direction must be synchronized when this happens).

OutputSynchronous

The CPU uses this bit to attempt to synchronize the output channel.

Acknowledged input sequence

This value is used for acknowledgment. The value of the input sequence counter is mirrored if the CPU has received a sequence successfully.

InputSynchronous

This bit acknowledges the synchronization of the input channel for the module. This indicates that the CPU is ready to receive data.

TxByte

See RxByte

7.3.7.2.1 X20AO2438-C0x

Register	Name	Bytes	Module			
			X20AO2438-C01		X20AO2438-C02	
Input:						
30	Reserved	1	Byte		Byte	
	Status of the output 1	1	Byte		Byte	
31	Reserved	1	Byte		Byte	
	Status of the output 2	1	Byte		Byte	
636	Value of the process variables 1 (HighWord) Channel 1	2	Word			
	Value of the process variables 1 (LowWord) Channel 1	2	Word			
641	Reserved	1	Byte			
	HART code 1 Channel 1	1	Byte			
660	Value of the process variables 2 (HighWord) Channel 1	2	Word			
	Value of the process variables 2 (LowWord) Channel 1	2	Word			
665	Reserved	1	Byte			
	HART code 2 Channel 1	1	Byte			
1148	Value of the process variables 1 (HighWord) Channel 2	2	Word			
	Value of the process variables 1 (LowWord) Channel 2	2	Word			
1153	Reserved	1	Byte			
	HART code 1 Channel 2	1	Byte			
1172	Value of the process variables 2 (HighWord) Channel 2	2	Word			
	Value of the process variables 2 (LowWord) Channel 2	2	Word			
1177	Reserved	1	Byte			
	HART code 2 Channel 2	1	Byte			
Output:						
0	Analog output 1	2		Word		Word
2	Analog output 2	2		Word		Word
Data bytes in DP frame			28 in	4 out	4 in	4 out

Support with firmware version ≥ V1.43

Status of the output

The status register gives the user feedback about whether the respective channel is functioning properly.

Bit	Name	Value	Information
0 - 1	Reserved	-	
2	Wiring	0	Line OK
		1	Open line
3	Conversion temperature	0	Conversion temperature OK
		1	Conversion temperature too high
4 - 6	Reserved	-	
7	Module supply	0	Module supply OK
		1	Module supply error

Value of the process variables

These registers return the current value of the process variable that has been read.

Information:

These registers are of data type REAL, which means that the available bytes on the X2X Link are filled more quickly when operated cyclically. If information from several slave nodes is needed, it must be retrieved acyclically or using FlatStream.

Data type	Values	Information
REAL	IEEE745 SPF	32-bit data type with valid value
	0x7FA00000	Not a number (NaN) with invalid value

HART code

These registers return a HART-specific code that specifies the unit for the measured value. The coding for this is established in the HART specification.

Values
See description of the HART slave See HART specification

Analog output

These registers provide the standardized output values. Depending on the scaling selected, the value range and the data type can be adapted to the requirements of the application. Once a permitted value is determined, the module outputs the respective current.

Information:

The value "0" disables the channel status LED.

Values
0 to 65,535

7.3.7.3 X20AOx622

Register	Name	Bytes	Module							
			X20AO2622		X20AO2622-C11		X20(c)AO4622		X20(c)AO4622-C11	
Output:										
0	Analog output 1	2		Word		Word		Word		Word
2	Analog output 2	2		Word		Word		Word		Word
4	Analog output 3	2						Word		Word
6	Analog output 4	2						Word		Word
18	Channel configuration	1		1)		2)		1)		2)
Data bytes in DP frame			0 in	4 out	0 in	4 out	0 in	8 out	0 in	8 out

1) The register can be modified in the parameter dialog box for the I/O module and is transferred acyclically.
2) The register is transferred acyclically. Mode 4 to 20 mA possible.

Analog output

These registers provide the standardized output values. Once a permitted value is received the module outputs the respective current or voltage.

Values	Information
-32,768 to 32,767	Voltage signal -10 to 10 VDC
0 to 32,767	Current signal 0 to 20 mA
0 to 32,767	Current signal 4 to 20 mA[1)]

1) From upgrade version 1.0.2.0 or hardware revision "I0"

Channel configuration

This register can be used to set the channel type of the outputs.

Each channel is capable of handling either current or voltage signals. The type of signal is determined by the connection terminals used. Since current and voltage require different adjustment values, it is also necessary to configure the desired type of output signal. The following output signals can be set:

- ±10 V voltage signal (default)
- 0 to 20 mA current signal
- 4 to 20 mA current signal (only "-C11" modules)

Bit	Name	Value	Information
0	Channel 1	0	Voltage signal
		1	Current signal, measurement range corresponding to bit 4
1	Channel 2	0	Voltage signal
		1	Current signal, measurement range corresponding to bit 5
2	Channel 3 or reserved	x	Like channel 1 or 0
3	Channel 4 or reserved	x	Like channel 1 or 0
4	Channel 1: Current measurement range	0	0 to 20 mA current signal
		1	4 to 20 mA current signal
5	Channel 2: Current measurement range	0	0 to 20 mA current signal
		1	4 to 20 mA current signal
6	Channel 3: Current measurement range or reserved	x	Like channel 1: Current measurement range or 0
7	Channel 4: Current measurement range or reserved	x	Like channel 1: Current measurement range or 0

7.3.7.4 X20AOx632 / X20AO4635

Register	Name	Bytes	Module			
			X20AO2632 X20AO2632-1		X20AO4632 X20AO4632-1 X20AO4635	
Output:						
2	Analog output 1	2		Word		Word
4	Analog output 2	2		Word		Word
6	Analog output 3	2				Word
8	Analog output 4	2				Word
0	Channel configuration	1		1)		1)
Data bytes in DP frame			0 in	4 out	0 in	8 out

1) The register can be modified in the parameter dialog box for the I/O module and is transferred acyclically.

Revision B0 or higher of the I/O module is required.

Analog output

These registers provide the standardized output values. Once a permitted value is received the module outputs the respective current or voltage.

Information:

The value "0" disables the channel status LED.

Values	
-32767 to 32767	Voltage
0 to 32,767	Current

Channel configuration

This register can be used to set the channel type of the outputs.

Each channel is capable of handling either current or voltage signals. The type of signal is determined by the connection terminals used. Since current and voltage require different adjustment values, it is also necessary to configure the desired type of output signal. The following output signals can be set:

- ±11 V voltage signal (default)
- 0 to 22 mA current signal

Bit	Description	Value	Information
0 - 7	Reserved	0	
8	Channel 1	0	Voltage signal
		1	Current signal
9	Channel 2	0	Voltage signal
		1	Current signal
10	Channel 3 or reserved	x	Like channel 1 or 0
11	Channel 4 or reserved	x	Like channel 1 or 0
10 - 15	Reserved	0	

7.3.8 Temperature modules

7.3.8.1 X20ATx222

Register	Name	Bytes	Module			
			X20AT2222		X20(c)AT4222	
Input:						
0	Temperature value input 1	2	Word		Word	
2	Temperature value input 2	2	Word		Word	
4	Temperature value input 3	2			Word	
6	Temperature value input 4	2			Word	
30	**HI:** 0 **LO:** Input status[1]	2	Word		Word	
Output:						
16	Filter parameter	1		[2]		[2]
18	Configure sensor type Channel 1 - 2	1		[2]		[2]
	Configure sensor type Channel 3 - 4	1				
Data bytes in DP frame			6 in	0 out	10 in	0 out

1) Diagnostics information is automatically sent to the PROFIBUS DP master.
2) The register is transferred acyclically.

The **Connection** parameter in the parameter dialog box of the I/O module can be used to select between a 2 or 3-wire connection. This enables the corresponding function model of the I/O module.

Temperature value input

This register is used to indicate the analog input values depending on the configured operating mode.

Values	Temperature/ resistance	Input signal
-2,000 to 8,500	For -200.0 to 850.0°C	PT100 sensor type
-2,000 to 8,500	For -200.0 to 850.0°C	PT1000 sensor type
1 to 45,000	Resolution 0.1 Ω	Resistance measurement 0.1 to 4500 Ω
1 to 45,000	Resolution 0.05 Ω	Resistance measurement 0.05 to 2250 Ω

In order for the user to always be supplied with a defined output value, the following must be taken into consideration:

- Up to the first conversion, 0x8000 is output.
- After switching the sensor type, 0x8000 is output until the first conversion.
- If the input is not switched on, 0x8000 is output.

Input status

The input channel status is indicated in this register. A change in the monitoring status generates an error message. This information is transferred with the cyclic data; a diagnostics message is also sent when an error occurs.

Bit	Description	Value	Information
0 - 1	Channel 1	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
2 - 3	Channel 2	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
4 - 5	Channel 3 (only X20AT4222)	x	Values same as channel 1
6 - 7	Channel 4 (only X20AT4222)	x	Values same as channel 1

Limiting the analog value

In addition to the status information, the analog value is set to the values listed below by default when an error occurs.

Error status	Temperature measurement Digital value for error	Resistance measurement Digital value for error
Open line	32767 (0x7FFF)	65535 (0xFFFF)
Upper limit value exceeded	32767 (0x7FFF)	65535 (0xFFFF)
Lower limit value exceeded	-32767 (0x8001)	0 (0x0000)
Invalid value	-32768 (0x8000)[1] 32767 (0x7FFF)[2] 65535 (0xFFFF)[3]	65535 (0xFFFF)

1) Default value or channel was disabled in the I/O configuration.
2) After switching off the channel during operation.
3) Value in function model 254 - Bus controller.

Filter parameter

The filter time of all analog inputs is defined in this register. The reciprocal (1 / converter rate) defines the filter time of all analog inputs; the conversion time for the channels depends on their usage. For the formulas listed in table "Conversion time", "n" corresponds to the number of channels that are switched on.

Value	Filter	Filter time
0	15 Hz	66.7 ms
1	25 Hz	40 ms
2	30 Hz	33.3 ms
3	50 Hz	20 ms
4	60 Hz	16.7 ms
5	100 Hz	10 ms
6	500 Hz	2 ms
7	1000 Hz	1 ms

Conversion time

Conversion time according to channel use	
1 channel	Corresponds to the filter time (= 1 / converter rate)
n channels with the same sensor type	n * (20 ms + filter time)
n channels with different sensor types	n * (20 ms + 2 * filter time)

Configure sensor type

This register is used to configure the sensor type for individual channels.

This module is designed for temperature and resistance measurement. The sensor type must be specified because of the different calibration values for temperature and resistance.

Bit	Name	Value	Information
0 - 3	Channel 1	0000 - 0001	Reserved
		0010	PT100 sensor type
		0011	PT1000 sensor type
		0100	Reserved
		0101	Resistance measurement 0.1 to 4500 Ω
		0110	Resistance measurement 0.05 to 2250 Ω
		1111	Channel disabled
4 - 7	Channel 2	0000 - 0001	Reserved
		0010	PT100 sensor type
		0011	PT1000 sensor type
		0100	Reserved
		0101	Resistance measurement 0.1 to 4500 Ω
		0110	Resistance measurement 0.05 to 2250 Ω
		1111	Channel disabled
8 - 11	Channel 3 (only X20AT4222)	x	Values same as channel 1
12 - 15	Channel 4 (only X20AT4222)	x	Values same as channel 1

The default setting for all channels is ON.

Any inputs that are not needed can be switched off, which reduces the I/O update time. Inputs can also be only switched off temporarily.

The amount of time saved can be calculated with the following formula. And "n" corresponds to the number of inputs that are switched off.

$$\text{Time saved} = n \cdot (20\ \text{ms} + \text{filter time})$$

Examples

Inputs are filtered using a 60 Hz filter.

	Example 1	Example 2	Example 3
Switched on inputs	1	1 and 3	1 to 4
Conversion time	16.7 ms	73.4 ms	146.8 ms

7.3.8.2 X20AT4232

Register	Name	Bytes	Module X20AT4232	
Input:				
0	Temperature value input 1	2	Word	
2	Temperature value input 2	2	Word	
4	Temperature value input 3	2	Word	
6	Temperature value input 4	2	Word	
30	**HI:** 0 **LO:** Input status[1)]	2	Word	
Output:				
16	Filter parameter	1		[2)]
18	Configure sensor type Channel 1 - 2	1		[2)]
	Configure sensor type Channel 3 - 4	1		
Data bytes in DP frame			10 in	0 out

1) Diagnostics information is automatically sent to the PROFIBUS DP master.
2) The register is transferred acyclically.

Temperature value input

This register is used to indicate the analog input values depending on the configured operating mode.

Values	Temperature/ resistance	Input signal
-300 to 1000	For -30.0 to 100.0°C	Sensor NTC10K type 1
-300 to 1000	For -30.0 to 100.0°C	Sensor NTC10K type 2
0 to 40,000	Resolution 5 Ω	Resistance measurement 0 to 200 kΩ

In order for the user to always be supplied with a defined output value, the following must be taken into consideration:

- Up to the first conversion, 0x8000 is output.
- After switching the sensor type, 0x8000 is output until the first conversion.
- If the input is not switched on, 0xFFFF is output.

Input status

The input channel status is indicated in this register. A change in the monitoring status generates an error message. This information is transferred with the cyclic data; a diagnostics message is also sent when an error occurs.

Bit	Description	Value	Information
0 - 1	Channel 1	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
...		...	
6 - 7	Channel 4	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line

Limiting the analog value

In addition to the status information, the analog value is set to the values listed below by default when an error occurs.

Error status	Temperature measurement Digital value for error	Resistance measurement Digital value for error
Open line	32767 (0x7FFF)	65535 (0xFFFF)
Upper limit value exceeded	32767 (0x7FFF)	65535 (0xFFFF)
Lower limit value exceeded	-32767 (0x8001)	0 (0x0000)
Invalid value	-32768 (0x8000)[1)] 32767 (0x7FFF)[2)] 65535 (0xFFFF)[3)]	65535 (0xFFFF)

1) Default value or channel was disabled in the I/O configuration.
2) After switching off the channel during operation.
3) Value in function model 254 - Bus controller.

Filter parameter

This register is used to configure the filter time for all analog inputs. The reciprocal (1 / converter rate) defines the filter time of all analog inputs; the conversion time for the channels depends on their usage. For the formulas listed in the table "Conversion time", "n" corresponds to the number of channels that are switched on.

Value	Filter	Filter time
0	15 Hz	66.7 ms
1	25 Hz	40 ms
2	30 Hz	33.3 ms
3	50 Hz (default)	20 ms
4	60 Hz	16.7 ms

Conversion time

Conversion time according to channel use	
1 channel	Corresponds to the filter time (= 1 / converter rate)
n channels with the same sensor type	n * (20 ms + filter time)
n channels with different sensor types	n * (20 ms + 2 * filter time)

Configure sensor type

This register is used to configure the sensor type for individual channels.

This module is designed for temperature and resistance measurement. The sensor type must be specified because of the different calibration values for temperature and resistance.

Bit	Name	Value	Information
0 - 3	Channel 1	0000	Sensor: NTC10K type 1[1)]
		0001	Sensor: NTC10K type 2[2)]
		0010 - 0011	Reserved
		0100	Channel switched off
		0101	Resistance measurement 0 to 200 kΩ
		0110	Reserved
		0111	Channel switched off
		1000 - 1111	Reserved
...		...	
12 - 15	Channel 4	0000	Sensor: NTC10K type 1[1)]
		0001	Sensor: NTC10K type 2[2)]
		0010 - 0011	Reserved
		0100	Channel switched off
		0101	Resistance measurement 0 to 200 kΩ
		0110	Reserved
		0111	Channel switched off
		1000 - 1111	Reserved

1) Sensor NTC10K type 1: Vishay NTCLE100E3103GB0, $B_{25/85}$ = 3977
2) Sensor NTC10K type 2: Vishay NTCLE413E2103F400L, $B_{25/85}$ = 3435

The default setting for all channels is ON.

Any inputs that are not needed can be switched off, which reduces the I/O update time. Inputs can also be only switched off temporarily.

The amount of time saved can be calculated with the following formula. And "n" corresponds to the number of inputs that are switched off.

$$\text{Time saved} = n \cdot (20\ \text{ms} + \text{filter time})$$

Examples

Inputs are filtered using a 60 Hz filter.

	Example 1	Example 2	Example 3
Switched on inputs	1	1 and 3	1 to 4
Conversion time	16.7 ms	73.4 ms	146.8 ms

7.3.8.3 X20AT23x1

Register	Name	Bytes	Module	
			X20AT2311 X20AT2321	
Input:				
0	Temperature value input 1	4	Long	
4	Temperature value input 2	4	Long	
30	**HI:** 0 **LO:** Input status[1)]	2	Word	
Output:				
2049	Filter parameter	1		[2)]
2051	Configure sensor type	1		[2)]
Data bytes in DP frame			6 in	0 out

1) Diagnostics information is automatically sent to the PROFIBUS DP master.
2) The register is transferred acyclically.

Temperature value input

These registers are used to indicate the analog input values depending on the configured operating mode.

Values	Temperature/ resistance	Input signal
-200,000 to +850,000	for -200°C to +850°C	**X20AT2311:** Sensor type PT100 **X20AT2321:** Sensor type PT1000
500 to 390,000	Resolution 0.001 Ω	**X20AT2311:** Resistance measurement resolution 0.5 Ω to 390 Ω **X20AT2321:** Resistance measurement resolution 0 to 3910 Ω

In order for the user to always be supplied with a defined output value, the following must be taken into consideration:

- Up to the first conversion, 0x80000000 is output.
- After switching the sensor type, 0x80000000 is output until the first conversion.
- If the input is not switched on, 0x80000000 is output.

Input status

The input channel status is indicated in this register. This information is transferred with the cyclic data; a diagnostics message is also sent when an error occurs.

Bit	Name	Value	Information
0 - 1	Channel 1	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
2 - 3	Channel 2	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
4 - 7	Reserved	0	

In addition to the status info, the error type also sets the analog value as follows:

Error status	Temperature measurement - Digital value for error	Resistance measurement - Digital value for error
Open line	+2147483647 (0x7FFFFFFF)	+4294967295 (0xFFFFFFFF)
Upper limit value exceeded	+2147483647 (0x7FFFFFFF)	+4294967295 (0xFFFFFFFF)
Lower limit value exceeded	-2147483647 (0x80000001)	-2147483647 (0x80000001)
Invalid value	-2147483648 (0x80000000)	-2147483648 (0x80000000)

Filter parameter

The filter time of all analog inputs is defined in this register.

Value	Filter	Filter time
0	15 Hz	66.7 ms
1	25 Hz	40 ms
2	30 Hz	33.3 ms
3	50 Hz	20 ms
4	60 Hz	16.7 ms
5	100 Hz	10 ms
6	500 Hz	2 ms
7	1000 Hz	1 ms
8	10 Hz	100 ms
9	5 Hz	200 ms
19	2.5 Hz	400 ms

Conversion time and resolution

The conversion time for the channels depends on the filter time set in the filter parameters.

Use of the channels	Conversion time
All channels regardless of configuration	1 x filter time

The following table shows the maximum frequency with which the specified resolution can be achieved.

Filter / Filter time	Resolution
5 Hz / 200 ms	0.001°C
50 Hz / 20 ms	0.01°C
1000 Hz / 1 ms	0.1°C

Configure sensor type

The sensor type of the individual channels is configured in this register.

This module is designed for temperature and resistance measurement. Due to different adjustment values for temperature and resistance, the sensor type must be selected.

All channels are switched on by default.

Bit	Name	Value	Information
0 - 3	Channel 1	0000	Reserved
		0001	Sensor type PT100/PT1000, resolution 1 mK[1)]
		0010	Resistance measurement 0.5 Ω to 390 Ω or 0 to 3910 Ω, resolution 1 mΩ[1)]
		0011 - 0110	Reserved
		0111	Channel disabled
		1xxx	Reserved
4 - 7	Channel 2	0000	Reserved
		0001	Sensor type PT100/PT1000, resolution 1 mK[1)]
		0010	Resistance measurement 0.5 Ω to 390 Ω or 0 to 3910 Ω, resolution 1 mΩ[1)]
		011 - 0110	Reserved
		0111	Channel disabled
		1xxx	Reserved

1) See Temperature value input.

7.3.8.4 X20ATx402

Register	Name	Bytes	Module			
			X20AT2402		X20(c)AT6402	
Input:						
0	Temperature value input 1	2	Word		Word	
2	Temperature value input 2	2	Word		Word	
4	Temperature value input 3	2			Word	
6	Temperature value input 4	2			Word	
8	Temperature value input 5	2			Word	
10	Temperature value input 6	2			Word	
	Filler byte	1	Word			
30	Input status 1 - 4[1]	1			Word	
31	Input status 5 - 6[1]	1				
Output:						
24	Filter parameter	1		[2]		[2]
26	Configure sensor type	1		[2]		[2]
27	Disabling channels	1		[2]		[2]
Data bytes in DP frame			6 in	0 out	14 in	0 out

1) Diagnostics information is automatically sent to the PROFIBUS DP master.
2) The register is transferred acyclically.

Temperature value input

Analog input value depending on the configured sensor type:

Values	Temperature	Input signal
-2,100 to +12,000	for -210°C to +1200°C	Type J (FeCuNi)
-2,700 to +13,720	for -270°C to +1372°C	Type K (NiCrNi)
-2,700 to +13,000	for -270°C to +1300°C	Type N (NiCrSi)
-500 to +17,680	for -50°C to +1768°C	Type S (PtRhPt)
0 to +18200	For 0°C to +1820.0°C	Type B (PtRhPt)
-500 to +16640	For -50.0°C to +1664.0°C	Type R (PtRhPt)
-32,768 to +32,767		Raw value without linearization and terminal temperature compensation: Resolution 1.0625 µV for a measurement range of ±35 mV
-32,768 to +32,767		Raw value without linearization and terminal temperature compensation: Resolution 2.125 µV for a measurement range of ±70 mV

In order for the user to always be supplied with a defined output value, the following must be taken into consideration:

- Up to the first conversion, 0x8000 is output.
- After switching the sensor type, 0x8000 is output until the first conversion.
- If the input is not switched on, 0x8000 is output.

Input status

The status of input channels 1 to 2 or 4 is indicated in this register. This information is transferred with the cyclic data; a diagnostics message is also sent when an error occurs.

Bit	Description	Value	Information
0 - 1	Channel 1	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
2 - 3	Channel 2	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
4 - 5	Channel 3 (only X20AT6402)	x	Values same as channel 1
6 - 7	Channel 3 (only X20AT6402)	x	Values same as channel 1

Input status

The status of input channels 5 and 6 is indicated in this register. This information is transferred with the cyclic data; a diagnostics message is also sent when an error occurs.

Bit	Description	Value	Information
0 - 1	Channel 5	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
2 - 3	Channel 6	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
4 - 7	Reserved	0	

In addition to the status info, the error type also sets the analog value as follows:

Error status	Temperature measurement Digital value for error	Resistance measurement Digital value for error
Open line	+32767 (0x7FFF)	65535 (0xFFFF)
Upper limit value exceeded	+32767 (0x7FFF)	65535 (0xFFFF)
Lower limit value exceeded	-32767 (0x8001)	0 (0x0000)
Invalid value	-32768 (0x8000)	65535 (0xFFFF)

Filter parameter

This register configures input filters and environmental conditions.

The filter time for all analog inputs is defined using the input filter parameter. The reciprocal (1 / converter rate) defines the filter time of all analog inputs; the conversion time for the channels depends on their usage. In table Conversion time, "n" corresponds to the number of switched-on channels.

Value	Filter	Filter time	Digital converter resolution
0	15 Hz	66.7 ms	16-bit
1	25 Hz	40 ms	16-bit
2	30 Hz	33.3 ms	16-bit
3	50 Hz	20 ms	16-bit
4	60 Hz	16.7 ms	16-bit
5	100 Hz	10 ms	16-bit
6	500 Hz	2 ms	16-bit
7	1000 Hz	1 ms	16-bit

Environmental conditions are set in order to adjust the internal terminal temperature characteristic curve to the type and amount of generated heat dissipated to the module.

This selection is based on the power consumption of the modules connected immediately to the left and right on the X2X Link. Power consumption values can also be found in the technical data for the corresponding module. The higher value is used for the configuration.

Bit	Description	Value	Information
0 - 3	Filter time	0000	15 Hz
		0001	25 Hz
		0010	30 Hz
		0011	50 Hz
		0100	60 Hz
		0101	100 Hz
		0110	500 Hz
		0111	1000 Hz
		1000 to 1111	Not permitted
4 - 7	Environmental conditions	0000	Default, no calculation for adjustment
		0001	Power dissipation less than 0.2 W
		0010	Power dissipation less than 1 W
		0011	Power dissipation more than 1 W
		0100 to 1111	Not permitted

Conversion time

The conversion time depends on the number of activated channels. For the formulas listed in the table, 'n' corresponds to the number of channels that are switched on.

Channel uses	Conversion time
n channels with different sensor types	(n + 1) * (2 * filter time + 200 µs)

Examples

Inputs are filtered using a 50 Hz filter.

	Example 1	Example 2
Switched on inputs	1	1 + 2
Input conversion times	40.2 ms	80.4 ms
Conversion time for the terminal temperature	40.2 ms	40.2 ms
Total conversion time	80.4 ms	120.6 ms

Configure sensor type

This module is designed for a wide range of sensor types. The sensor type must be configured because of the different alignment values. This parameter simultaneously applies to all channels.

Values	Information
0	Conversion switched off
1	Sensor type J
2	Sensor type K
3	Sensor type S
4	Sensor type N
5	Conversion switched off
6	Raw value without linearization and terminal temperature compensation: Resolution 1.0625 µV for a measurement range of ±35 mV
7	Raw value without linearization and terminal temperature compensation: Resolution 2.125 µV for a measurement range of ±70 mV
8 - 63	Conversion switched off
64	Sensor type R
65 - 71	Conversion switched off
72	Sensor type B
73 - 255	Conversion switched off

Disabling channels

By default, all channels are switched on. To save time, individual channels can be switched off. Time savings = (n + 1) * (200 µs + 2 * filter time), where 'n' is the number of disabled inputs.

Bit	Description	Value	Information
0	Channel 1	0	Off
		1	On
1	Channel 2	0	Off
		1	On
2 - 5	Channel 3 to 6 (only X20AT6402)	x	Values same as channel 1
2 or 6 - 7	Reserved	0	

Filler byte

These modules provide an extra input byte with zeros (padding). This supports master systems with word alignment.

7.3.8.5 X20ATx312

Register	Name	Bytes	Module			
			X20ATA312		X20ATB312	
Input:						
0	Temperature value input 1	4	Long		Long	
4	Temperature value input 2	4	Long		Long	
8	Temperature value input 3	4			Long	
12	Temperature value input 4	4			Long	
30	**HI:** - **LO:** Input status[1)]	2	Word		Word	
Output:						
130	Conversion rate	2		[2)]		[2)]
134	A/D operating mode	2		[2)]		[2)]
514	Channel parameters Channel 1	2		[2)]		[2)]
578	Channel parameters Channel 2	2		[2)]		[2)]
642	Channel parameters Channel 3	2				[2)]
706	Channel parameters Channel 4	2				[2)]
Data bytes in DP frame			10 in	0 out	18 in	0 out

1) Diagnostics information is automatically sent to the PROFIBUS DP master.
2) The register is transferred acyclically.

Support with firmware version ≥ V1.43

Temperature value input

If the channel is configured for resistance measurement, the current resistance value is made available in this register. If the channel is configured for temperature measurement, the current temperature value is made available in this register.

Values	Information
0 to 4,294,967,295	For resistance measurement
-2,147,483,648 to 2,147,483,647	For temperature measurement

Input status

The register bits are set if an error has been diagnosed and the error remains longer than the preconfigured delay.

Bit	Name	Value	Information
0	Underflow monitoring	0	No error
		1	Value below the permitted range
1	Overflow monitoring	0	No error
		1	Value above the permitted range
2	Sensor status	0	No error
		1	Sensor is not connected correctly
3	Reserved	-	
4	A/D converter	0	No error
		1	Invalid A/D converter output
5	Composite error	0	No error
		1	Composite error
6	Channel parameters	0	No error
		1	The Channel parameters register is faulty.
7	Power supply	0	No error
		1	The voltage supply (I/O) is faulty

Conversion rate

This register can be used to set the conversion rate for the Analog/Digital converter.

Values
5 to 1,023

Information:

The lower the conversion interval is set, the more precisely the value can be converted. However, this also increases the I/O update time.

A/D operating mode

This register can be used to set the operating mode for the Analog/Digital converter.

The individual options allow faster digitalization of the analog values, but this also reduces the precision of the measured values. The default value is 0.

Bit	Name	Value	Information
0	Chopper mode	0	Alternating amplification of the analog value
		1	Chopper mode off
1	Order of the SINC filter	0	SINC4
		1	SINC3
2 - 15	Reserved	-	-

The following applies:

ConversionTime(SINC3) = ConversionTime(SINC4) - 1 x ConversionCycle
ConversionTime(without Chop) = 0.5 x ConversionTime(Chop)

Channel parameters

This register defines the basic behavior of the channel.
The default value is 0x81.

Bit	Name	Value	Information
0 - 2	Sensor type with unit and resolution	001	PT100 [10 mK/bit] - Temperature measurement
		010	PT100 [1 mΩ/bit] - Resistance measurement
		011 to 111	Reserved
3 - 4	Reserved	-	
5	Replacement value strategy	0	Replace statically
		1	Retain last valid value
6	Monitoring the user-defined limit values	0	Switch off additional limits
		1	Switch on additional limits
7	Channel (on/off)	0	Switch off the entire channel
		1	Switch on the channel
8 - 15	Reserved	-	

7.3.8.6 X20ATA492

Register	Name	Bytes	Module X20ATA492	
Input:				
0	Temperature value input 1	2	Word	
2	Temperature value input 2	2	Word	
31	Input status 2	1	Word	
30	Input status 1	1		
Output:				
386	Channel configuration 1	2		1)
426	Channel configuration 2	2		1)
Data bytes in DP frame			6 in	0 out

1) The register is transferred acyclically.

Temperature value input

Analog input value depending on the configured sensor type:

Values	Temperature	Input signal
2,100 to 12,000	For -210 to 1200°C	Type J (Fe-CuNi)
-2,700 to 13,720	For -270 to 1372°C	Type K (NiCr-Ni)
-2,700 to 12,980	For -270 to 1298°C	Type N (NiCrSi-NiSi)
-500 to 17,680	For -50 to 1768°C	Type S (PtRh10-Pt)
-500 to 17,600	For -50 to 1760°C	Type R (PtRh13-Pt)
0 to 23,100	For 0 to 2310°C	Type C (WRe5-WRe26)
-2,700 to 4,000	For -270 to 400°C	Type T (Cu-CuNi)
0 to 18,200	For 0 to 1820°C	Type B (PtRh30-PtRh6)
-2,700 to 9,970	For -270 to 997°C	Type E (NiCr-CuNi)
-32,768 to 32,767		Voltage without linearization and terminal temperature compensation Resolution 1.0625 µV for a measurement range of ±35 mV
-32,768 to 32,767		Voltage without linearization and terminal temperature compensation Resolution 2.125 µV for a measurement range of ±70 mV

In order for the user to always be supplied with a defined output value, the following must be taken into consideration:

- Up to the first conversion, 0x8000 is output.
- After switching the sensor type, 0x8000 is output until the first conversion.
- If the input is switched off, 0x8000 is output.
- If an I/O voltage supply failure occurs, 0x8000 is output

Input status

The module's temperature inputs are monitored. A change in the monitoring status generates an error message. Some error information is only enabled after a configurable delay [ms] (as with the composite error) or after a configurable delay as a multiple of the conversion cycle when underflow, overflow or open lines occurs. This information is transferred with the cyclic data; a diagnostics message is also sent when an error occurs.

Bit	Name	Value	Information
0	Underflow monitoring	0	No error
		1	Underflow
1	Overflow monitoring	0	No error
		1	Overrun
2	Open line monitoring	0	No error
		1	Open line
3	Composite message: Terminal temperature measurement error	0	No error
		1	Error during terminal temperature measurement
4	Conversion monitoring	0	No error
		1	Conversion error
5	Composite error monitoring	0	No error
		1	Composite error
6	Configuration monitoring	0	No error
		1	The Channel configuration register is faulty.
7	Monitoring of the I/O supply	0	No error
		1	I/O supply error

In addition to the status info, the error type also sets the analog value as follows:

Error status	Digital value for error
Open line	32767 (0x7FFF)
Upper limit value exceeded	32767 (0x7FFF)
Lower limit value exceeded	-32767 (0x8001)
Invalid value or I/O supply error	-32768 (0x8000)

Channel configuration

These registers are used to set the configuration accordingly for temperature channel and cold junction measurement 01 and 02.

Bit	Name		Information
0 - 5	Defines sensor	000000	Sensor type J (default)
		000001	Sensor type K
		000010	Sensor type N
		000011	Sensor type S
		000100	Sensor type R
		000101	Sensor type C
		000110	Sensor type T
		000111	Sensor type B
		001000	Sensor type E
		111101	Voltage without linearization and terminal temperature compensation Resolution 1.0625 µV for a measurement range of ±35 mV
		111110	Voltage without linearization and terminal temperature compensation Resolution 2.125 µV for a measurement range of ±70 mV
6 - 7	Selection of temperature model	00	Horizontal installation, low thermal radiance ≤1 W
		01	Horizontal installation, high thermal radiance >1 W
		10	Vertical installation, low thermal radiance ≤1 W
		11	Vertical installation, high thermal radiance >1 W
8 - 9	Cold junction type	00	Cold junction sensor PT1000
		01	Reserved
		10	Reserved
		11	Cold junction conversion disabled
10	Unit for cold junction value	0	Standardization / display 0.1°C
		1	Standardization / display 0.1 Ω
11	Cold junction value input	0	Measurement of the internal cold junction
		1	External specific via analog output value
12	Internal terminal compensation according to temperature model	0	Mode disabled
		1	Internal compensation mode according to the configured temperature model(see Bits 6 and 7)
13	Replacement value strategy	0	Use replacement values if error occurs
		1	Keep the last valid converted value
14	User limit value monitoring[1)]	0	User limit value monitoring disabled
		1	User limit value monitoring enabled
15	Channel activation	0	Channel disabled
		1	Channel enabled

1) Signal monitoring and generation of error states for underflow, overflow and open line are already automatically enabled on the module; however, the user limit values are not applied until bit 14 is set. Likewise, the replacement value strategy is only enabled if this bit is set.

If this mode is selected, it is important to make sure that both PT1000 cold junction sensors are configured and connected!

This setting is used to adjust the internal terminal temperature characteristic curve to the type and amount of generated heat dissipated to the module. This selection is based on the power consumption of the modules connected immediately to the left and right on the X2X Link. This data can be found in the modules' data sheet. The higher value is used for the configuration.

7.3.8.7 X20ATC402

Register	Name	Bytes	Module X20ATC402	
Input:				
0	Temperature value input 1	2	Word	
2	Temperature value input 2	2	Word	
4	Temperature value input 3	2	Word	
6	Temperature value input 4	2	Word	
8	Temperature value input 5	2	Word	
10	Temperature value input 6	2	Word	
30	Input status 1 - 4	2	Word	
31	Input status 5 - 6			
Output:				
770	External temperature compensation 1	2		Word
774	External temperature compensation 2	2		Word
778	External temperature compensation 3	2		Word
782	External temperature compensation 4	2		Word
786	External temperature compensation 5	2		Word
790	External temperature compensation 6	2		Word
Data Bytes in DP Frame			14 in	12 out

Support with firmware version ≥ V1.43

Temperature value input

This register is used to indicate the analog input values depending on the configured sensor type.

Values	Temperature	Input signal
-2,100 to 12,000	For -210 to 1200°C	Type J (Fe-CuNi)
-2,700 to 13,720	For -270 to 1372°C	Type K (NiCr-Ni)
-2,700 to 12,980	For -270 to 1298°C	Type N (NiCrSi-NiSi)
-500 to 17,680	For -50 to 1768°C	Type S (PtRh10-Pt)
-500 to 17,600	For -50 to 1760°C	Type R (PtRh13-Pt)
0 to 23,100	For 0 to 2310°C	Type C (WRe5-WRe26)
-2,700 to 4,000	For -270 to 400°C	Type T (Cu-CuNi)
0 to 18,200	For 0 to 1820°C	Type B (PtRh30-PtRh6)
-2,700 to 9,970	For -270 to 997°C	Type E (NiCr-CuNi)
-32,768 to 32,767		Voltage without linearization and terminal temperature compensation Resolution 1.0625 µV for a measurement range of ±35 mV
-32,768 to 32,767		Voltage without linearization and terminal temperature compensation Resolution 2.125 µV for a measurement range of ±70 mV

In order for the user to always be supplied with a defined output value, the following must be taken into consideration:

- Up to the first conversion, 0x8000 is output.
- After switching the sensor type, 0x8000 is output until the first conversion.
- If the input is switched off, 0x8000 is output.
- If an I/O voltage supply failure occurs, 0x8000 is output

Input status

The status of input channels 1 to 4 is indicated in this register.

Bit	Name	Value	Information
0 - 1	Channel 1	00	No error
		01	Underflow (lower value limit violated)
		10	Overflow (upper value limit violated)
		11	Open line
...	...	...	
6 - 7	Channel 4	00	No error
		01	Underflow (lower value limit violated)
		10	Overflow (upper value limit violated)
		11	Open line

Input status

The status of input channels 5 and 6 is indicated in this register.

Bit	Name	Value	Information
0 - 1	Channel 5	00	No error
		01	Underflow (lower value limit violated)
		10	Overflow (upper value limit violated)
		11	Open line
2 - 3	Channel 6	00	No error
		01	Underflow (lower value limit violated)
		10	Overflow (upper value limit violated)
		11	Open line
4 - 7	Reserved	-	

External temperature compensation

With external compensation, there is no need for internal conversion of the PT1000 values in the module. Instead, the reference temperatures have to be pre-processed in the program before being stored in the module.

This register can be used to send an externally generated compensation value from the PLC program to the module. There is a separate register for each temperature channel.

Values	Information
-32767 to 32767	In increments of 0.1°C.

7.3.9 Communication modules

7.3.9.1 X20CS1011

Register	Name	Bytes	Module			
			X20CS1011-C01		X20CS1011-C02	
Input:						
0	Input data 1 - 2	2	Word		Word	
2	Input data 3 - 4	2	Word		Word	
4	Input data 5 - 6	2	Word		Word	
6	Input data 7 - 8	2	Word		Word	
8	Input data 9 - 10	2	Word		Word	
10	Input data 11 - 12	2	Word		Word	
12	Input data 13 - 14	2	Word		Word	
14	Input data 15 - 16	2	Word		Word	
66	Status of the slave	2			Word	
70	Status of the master	2			Word	
77	**HI:** 0 **LO:** Master operating state	2			Word	
Output:						
16	Transferring control bits 1 - 4	2		Word		Word
18	Transferring control bits 5 - 8	2		Word		Word
20	Transferring control bits 9 - 12	2		Word		Word
22	Transferring control bits 13 - 16	2		Word		Word
Data bytes in DP frame			16 in	8 out	22 in	8 out

Support with firmware version ≥ V1.43

Input data

Each slave sends its input data and/or its status to the master.

The data volume consumes 1 byte per slave. Each slave has one diagnostics bit, which it sends to the master with the cyclic data. This bit is a message bit if an application error occurs (on the module). It is always located in the highest value bit.

The master can constantly evaluate this bit. The diagnostic bit is set on the slave if the status of the slave is "Error". Slaves that do not have any input data will still send a byte that is used to make their status data available. This is required because the master also monitors the slaves for proper functionality through the receipt of this byte.

Bit	Description	Value	Information
0	Input state - Digital input 1	0 or 1	
...		...	
3	Input state - Digital input 4	0 or 1	
4 - 6	Reserved	0	
7	Error status	0	No error on the slave
		1	Error on the slave

Status of the master

The current status information for the master is .

Bit	Description	Value	Information
0	LIN_BUS_SETUP_COMPLETE	0	Saved configuration does not match the actual hardware on the bus
		1	Setup finished: SCAN or SETUP after config button is valid
1	LIN_FATAL_ERROR	0	No error on the bus
		1	SmartWire bus is defective: e.g. short circuit, no echo →more than 10 consecutive communication errors have occurred. **Information:** **The failure of a slave is not a communication error. Instead it is indicated in the slave status and the scheduler continues to run!**
2	LIN_MASTER_PREOP	0	SmartWire stack not in PREOP mode
		1	SmartWire stack in PREOP mode
3	LIN_MASTER_OP	0	SmartWire stack not in OP mode
		1	SmartWire stack in OP mode
4	LIN_GLOBAL_CONTROL	0	No command sent
		1	Set SmartWire stack to OP mode: Bit is written to the enable bit and can be read back
5	Reserved	0	
6	LIN_POWER_SUPPLY_STATE	0	Bus voltage supply is not OK
		1	Bus voltage supply is OK
7	Reserved	0	
8	DP_CHECK_COMPLETED	0	Not a valid configuration
		1	Configuration check completed (Not Used) (could optionally be written by the PLC, if the SCAN (configuration) is OK and was able to be read back from here)
9	Reserved	0	
10	DP_RECONFIGURATION	0	X2X reconfiguration →X2X configuration button not pressed
		1	X2X reconfiguration →X2X configuration button can be read back
11 - 15	Reserved	0	

The register receives the following value after successfully starting:

Equal to the decimal value: 345

Bit	Description	Value	Information
0	LIN_BUS_SETUP_COMPLETE	1	SmartWire setup complete: SCAN or SETUP after config button is valid
3	LIN_MASTER_OP	1	SmartWire stack in OP mode
4	LIN_GLOBAL_CONTROL	1	Set SmartWire stack to OP mode - Command set
6	LIN_POWER_SUPPLY_STATE	1	Bus voltage supply is OK
7	DP_CHECK_COMPLETED	1	Configuration is OK

Status of the slave

The current state of the slave is indicated collectively in this register.

In the event of an error, the failed slaves are indicated in the respective bits.

Data is exchanged cyclically as long as none of these bits are set. If an error does error, then I/O transfer is stopped. The bus can be started again after the error has been corrected or a setup has been performed again.

Bit	Description	Value	Information
0	Slave 1	0	OK
		1	Errors
...		...	
15	Slave 16	0	OK
		1	Errors

Master operating state

The current state of the master state machine is indicated in this register.

Values	Code	Description
1	CHECK_INT_FRAM	Init State
2	CHECK_LIN_SUPPLY	Waiting for 17 V voltage OK
3	SET_TRANSCEIVER_MODE	Turn on transceiver
4	RESET_UART UART	Reset
6	INIT_LIN_SCAN	Init before bus scan
7	RUN_LIN_SCAN	Bus scan is running
8	WAIT_FOR_PUSHBUTTON	Scan != Configuration, waiting for Config button
9	TIME_DELAY	Delay before bus setup
10	INIT_LIN_SETUP	Init before bus setup
11	RUN_LIN_SETUP	Bus setup is running (new configuration)
12	DP_CFG_CHECK	PLC has set "Wait for configuration"
15	SET_SLAVES_TO_OP	Sets slaves to OP mode (after successful scan or setup)
16	SET_SLAVES_TO_PREOP	Sets slaves to PREOP mode (after errors have occurred, before LIN_ERROR or INT_ERROR)
19	INIT_LIN_SCHED	Init bus scheduling
20	RUN_LIN_SCHED	Bus scheduler is running
21	LIN_ERROR_STATE	A fatal bus error has occurred (permanent)
22	INT_ERROR_STATE	A fatal internal error has occurred (permanent)
23	IDLE_STATE	Idle because there is no slave connected (permanent)

Transferring control bits

In these registers, the control bits are transferred to 2 consecutive slaves. Each slave receives 4 control bits, that must be selected from the 8 data bytes depending on the node address (1 to 16). These 4 control bits are assigned fixed values and utilization of the bits by the slave is optional.

All of the slaves evaluate this telegram. It must be sent cyclically by the master so that the slaves can ensure that the master is still functioning without any problems within the monitoring time (lifeguarding time = 400 ms).

Bit	Description	Value	Information
0	Slave N	0	Digital output 1 reset
		1	Digital output 1 set
...		..	
3	Slave N	0	Digital output 4 reset
		1	Digital output 4 set
4	Slave N + 1	0	Digital output 1 reset
		1	Digital output 1 set
...		..	
7	Slave N + 1	0	Digital output 4 reset
		1	Digital output 4 set

7.3.9.2 X20CS1013

Register	Name	Bytes	Module X20CS1013	
Input:				
258	DALI status	2	Word	
263	DALI message counter	1	Byte	
261	DALI response counter	1	Byte	
265	DALI response	1	Byte	
Output:				
257	Enabling/Disabling DALI	1		Byte
262	DALI control	2		Word
265	DALI address	1		Byte
267	DALI command	1		Byte
Data bytes in DP frame			6 in	6 out

Support with firmware version ≥ V1.43

DALI status

This register contains the current state of the DALI network.

Bit	Name	Value	Information
0	Enables/Disables the level converter	0	Communication off
		1	Communication on
1	Status of the last request	0	Valid request not yet sent
		1	Transmit procedure successful
2	Status of the last response	0	No response since the last request
		1	Receive procedure successful
3	Collision (multi-master)	0	No collision
		1	Collision in the DALI network
4 - 7	Reserved	-	
8	Transmit error	0	No error
		1	Transmit procedure failed
9	Receive error	0	No error
		1	Invalid response received
10 - 15	Reserved	-	

DALI message counter

This register provides the user with information about how many DALI messages have already been sent by the module.

Values
0 to 255

DALI response counter

This register provides the user with information about how many DALI messages have already been received by the module.

Values
0 to 255

DALI response

This register provides the user with access to the last valid response from the downstream DALI network.

Values
0 to 255

Enabling/Disabling DALI

This register is used to enable or disable the communication channel.

Bit	Name	Value	Information
0	Switches communication on or off (on the software side)	0	Switches the communication channel off
		1	Switches the communication channel on
1	Switches the energy saving mode on or off	0	Supplies the DALI network
		1	Switches the internal power supply unit for the module off
2 - 7	Reserved	-	

Information:

The module-internal power supply unit must be switched on for communication in the DALI network.

DALI control

This register is used to control the module. The respective command is transported via X2X Link and then executed by the module. The register is edge-triggered (i.e. this type of command is only triggered if the state of the respective bit changes).

Bit	Name	Value	Information
0	Requests command (pos. edge)	0	No action
		1	Transmits request in the DALI network
1	Reserved	-	
2	Acknowledges the status byte (pos. edge)	0	No action
		1	Resets the status byte
3	Acknowledges the transmission counter (pos. edge)	0	No action
		1	Resets the transmission counter
4	Acknowledges the response counter (pos. edge)	0	No action
		1	Resets the response counter
5 - 15	Reserved	-	

DALI address

This register provides the user with access to the last valid response from the downstream DALI network.

Values
0 to 255

DALI command

This register provides the module with the command for the addressed receiver(s) in the DALI network.

Values	Information
0 to 255	DALI or slave-specific command

Direct DALI commands (ARC)

These commands can be used to directly set the brightness of each DALI slave. The statements 1 to 254 correspond to a brightness of the connected DALI slave based on the following formula:

$$P = 10^{\frac{\text{Value} - 1}{253 / 3}} * \frac{P_{max}}{1000}$$

Command 0 can also be transmitted to switch off a DALI slave. In this case, the brightness decreases slowly at first and then shuts off when a critical power level is crossed.

Command 255 serves as an internal mask value. It is not applied by the DALI slave, which means it has no effect on its behavior.

Indirect DALI commands for lamp wattage

Indirect commands make digital communication possible on the DALI network. In addition to the commands defined in the DALI standard, some manufacturers of DALI slaves also define their own commands.

Selected standardized DALI commands

Source: EN 62386-102:2009

Code (dec.)	Function
Indirect control commands	
0	Switches off the light immediately – No smooth transition
1	200 ms dimming up – Possible to configure the dimming speed separately – No further change once maximum is reached – Command ignored when light is off
2	200 ms dimming down – Possible to configure the dimming speed separately – No further change once minimum is reached – Command does not turn light off
3	Increases the brightness by one step – No smooth transition – No further change once maximum is reached – Command ignored when light is off

Code (dec.)	Function
4	Decreases the brightness by one step – No smooth transition – No further change once minimum is reached – Command does not turn light off
5	Maximum brightness – No smooth transition – Turns the light on
6	Minimum brightness – No smooth transition – Turns the light on
7	Decrease brightness by one step (including switching off) – No smooth transition – Command can turn light off
8	Increase brightness by one step (including switching on) – No smooth transition – Switches on a switched-off light
9	Commence DACP sequence – Starts direct power control – Dimming speed adjusted dynamically by the control device – DACP sequence required at the end
10 - 15	Reserved
16 - 31	Enables scene 0 to 15 – Power regulated to the level stored in the scene

Indirect DALI commands for configuration

Indirect commands make digital communication possible on the DALI network. In addition to the commands defined in the DALI standard, some manufacturers of DALI slaves also define their own commands.

Information:

Some indirect DALI commands must be repeated within 100 ms. The module does not evaluate specified addresses and commands, which means this repetition must be ensured by the application.

Selected standardized DALI commands

Source: EN 62386-102:2009

Code (dec.)	Function	Response
Configuration commands[1)]		
32	Resets nonvolatile memory – DALI slave requires up to 300 ms for execution	
33	Reads out the current power level – Stores the current power value in the DTR – Command code 152 required	
34 - 41	Reserved	
Save DTR value[1)]		
42	Save as maximum power value	
43	Save as minimum power value	
44	Save power value as value for event of error	
45	Save power value as switch-on value	
46	Save value as dimming time	
47	Save value as dimming speed	
48 - 63	Reserved	
Used for setting system parameters[1)]		
64 - 79	Save DTR value as selected scene 0 to 15 – Scene number = Command number - 64	
80 - 95	Removes DALI slave from scene 0 to 15 – Scene number = Command number - 80	
96 - 111	Adds DALI slave to group 0 to 15 – Group number = Command number - 96	
112 - 127	Removes DALI slave from group 0 to 15 – Group number = Command number - 112	
128	Save DTR value as short address	
129 - 143	Reserved	
Request commands		
144	Checks the general status	**Bit / Value / Function** 0 / 0 / DALI slave status OK 0 / 1 / DALI slave status not OK 1 / 0 / Light status OK 1 / 1 / Light status not OK 2 / 0 / Light off 2 / 1 / Light on 3 / 0 / Last requested power level permissible 3 / 1 / Last requested power level not permissible 4 / 0 / Last dimming procedure complete 4 / 1 / Dimming procedure not yet complete 5 / 0 / DALI slave not in reset state 5 / 1 / DALI slave in reset state 6 / 0 / DALI slave has short address 6 / 1 / DALI slave has no short address 7 / 0 / Reset or control command not yet received by DALI slave 7 / 1 / Reset or control command received by DALI slave
145	Checks communication readiness	Yes/No
146	Checks for light failure	Yes/No
147	Checks whether light is currently on	Yes/No
148	Checks whether the last requested power value was applied	Yes/No
149	Checks whether the DALI slave is in reset state	Yes/No
150	Checks whether the DALI slave has a short address	Yes/No
151	Checks whether the DALI slave has a version number	The response depends on the DALI slave: • Yes/No (DALI slave has a version number or not) • Version number
152	Checks the DTR value	DTR value
153	Checks the device type	DALI-specific code for categorizing DALI slaves
154	Checks the physical minimum level (greater than 0)	Value of physical minimum level
155	Checks for power failure	Yes/No
156 - 159	Reserved	

Code (dec.)	Function	Response
160	Checks the current power level	Current power level or 255 if the light is being warmed up
161	Checks the maximum value	Maximum value
162	Checks the minimum value	Minimum value
163	Checks the switch-on power level	Switch-on power level
164	Checks the power level in the event of error	Power level in the event of error
165	Checks the dimming time and dimming speed	**Bit** / **Function** 0 - 3 / Dimming speed 4 - 7 / Dimming time
166 - 175	Reserved	
176 - 191	Checks the light level for scene 0 to 15	
192	Checks whether the DALI slave member is part of group 0 to 7	**Bit** / **Value** / **Function** 0 / 0 / Slave not in group 0 1 / Slave in group 0 ... 7 / 0 / Slave not in group 7 1 / Slave in group 7
193	Checks whether the DALI slave member is part of group 8 to 15	**Bit** / **Value** / **Function** 0 / 0 / Slave not in group 8 1 / Slave in group 8 ... 7 / 0 / Slave not in group 15 1 / Slave in group 15
194	Checks a 24-bit random address (H)	Random address (higher 8 bits)
195	Checks a 24-bit random address (M)	Random address (middle 8 bits)
196	Checks a 24-bit random address (L)	Random address (lower 8 bits)
197 - 223	Reserved	
224 - 255	Checks application-specific defined commands	

1) Any command in the range 32 to 129 must be repeated within the next 100 ms. No other commands can be transmitted to the DALI slave being addressed during this time.

7.3.9.3 X20CS1020 / X20CS1030

Register	Name	Bytes	Module					
			X20CS1020-C01 X20CS1030-C01		X20CS1020-C21 X20CS1030-C21		X20CS1020-C41 X20CS1030-C41	
Input:								
128	Input sequence	1	Byte		Byte		Byte	
129	RxByte 0	1	Byte		Byte		Byte	
130	RxByte 1	1	Byte		Byte		Byte	
131	RxByte 2	1	Byte		Byte		Byte	
...	[2]	1			Byte		Byte	
145	RxByte 16	1			Byte		Byte	
...	[3]	1					Byte	
157	RxByte 28	1					Byte	
Output:								
160	Output sequence	1		Byte		Byte		Byte
161	TxByte 0	1		Byte		Byte		Byte
162	TxByte 1	1		Byte		Byte		Byte
163	TxByte 2	1		Byte		Byte		Byte
...	[4]	1				Byte		Byte
177	TxByte 16	1				Byte		Byte
...	[5]	1						Byte
189	TxByte 28	1						Byte
12	Baud rate	1		[6]		[6]		[6]
1	Type of interface[7]	1		[6]		[6]		[6]
3	Number of data bits	1		[6]		[6]		[6]
5	Number of stop bits	1		[6]		[6]		[6]
7	Type of parity bit	1		[6]		[6]		[6]
229	FlatStream mode	1		[6]		[6]		[6]
74	Receive timeout	1		[6]		[6]		[6]
106	Transmit timeout	1		[6]		[6]		[6]
Data bytes in DP frame			4 in	4 out	18 in	18 out	30 in	30 out

2) Register 132 to Register 144 →RxByte 3 to RxByte 15
3) Register 146 to Register 156 →RxByte 17 to RxByte 27
4) Register 164 to Register 176 →TxByte 3 to TxByte 15
5) Register 178 to Register 188 →TxByte 17 to TxByte 27
6) The register can be modified in the parameter dialog box for the I/O module and is transferred acyclically.
7) Only module X20CS1030.

Support with firmware version ≥ V1.43

Input sequence

This register contains information about the communication status of the module. It is written by the module and should only be read by the CPU.

Bit	Name	Value	Information
0 - 2	Input sequence counter	0 to 7	Counter for sequences issued in the input direction
3	InputSynchronous	0	Not ready (disabled)
		1	Ready (enabled)
4 - 6	Acknowledged output sequence	0 to 7	Mirrors the output sequence counter value
7	OutputSynchronous	0	Not ready (disabled)
		1	Ready (enabled)

Input sequence counter

The input sequence counter is a continuous counter of sequences that have been issued by the module. The module uses the input sequence counter to direct the CPU to accept a sequence (the input direction must be synchronized when this happens).

InputSynchronous

The module uses this to attempt to synchronize the input channel.

Acknowledged output sequence

This value is used for acknowledgment. The value of the output sequence counter is mirrored if the module has received a sequence successfully.

OutputSynchronous

This bit acknowledges the synchronization of the output channel for the CPU. This indicates that the module is ready to receive data.

RxByte

The Tx and Rx bytes are cyclic registers used to transport the payload data and the necessary control bytes.
In the user program, only the Tx and Rx bytes from the CPU can be used. The corresponding counterparts are located in the module and are not accessible to the user. For this reason, names were chosen from the CPU point of view.

- "T" - "Transmit" →CPU *transmits* data to the module.
- "R" - "Receive" →CPU *receives* data from the module.

Values
0 to 65,535

Output sequence

This register contains information about the communication status of the CPU. It is written by the CPU and read by the module.

Bit	Name	Value	Information
0 - 2	Output sequence counter	0 to 7	Counter for sequences issued in the output direction
3	OutputSynchronous	0	Output direction disabled
		1	Output direction enabled
4 - 6	Acknowledged input sequence	0 to 7	Mirrors the input sequence counter value
7	InputSynchronous	0	Input direction not ready (disabled)
		1	Input direction ready (enabled)

Output sequence counter

The output sequence counter is a continuous counter of sequences that have been issued by the CPU. The CPU uses the output sequence counter to direct the module to accept a sequence (the output direction must be synchronized when this happens).

OutputSynchronous

The CPU uses this bit to attempt to synchronize the output channel.

Acknowledged input sequence

This value is used for acknowledgment. The value of the input sequence counter is mirrored if the CPU has received a sequence successfully.

InputSynchronous

This bit acknowledges the synchronization of the input channel for the module. This indicates that the CPU is ready to receive data.

TxByte

See RxByte

Baud rate

This register sets the baud rate of the interface in bit/s.

Values	Function
1200	1.2 kbaud
2400	2.4 kbaud
4800	4.8 kbaud
19200	19.2 kbaud
38400	38.4 kbaud
57600	57.6 kbaud
115200	115.2 kbaud

Type of interface

Register only exists in the X20CS1030 module.

This register is used to determine the current operating mode of the interface.

Enabling the interface is only permitted after complete configuration of the other registers. If parameters need to be changed, the interface must first be disabled.

Values	Function
0	Interface disabled (default)
4	RS422 interface enabled[1)]
5	RS422 interface enables as a bus[2)]
6	RS485 interface enabled with echo
7	RS485 interface enabled without echo

1) Connection between 2 stations
2) Connections between multiple stations possible. Transmit lines connected as with RS485 TriState.

Number of data bits

This register is used to specify the number of bits to be transferred for each character.

Values	Function
7	7 data bits
8	8 data bits (default)

Number of stop bits

This register is used to define the number of stop bits.

Values	Function
2	1 stop bit (default)
4	2 stop bits

Type of parity bit

This register is used to define the parity check type. Possible values are ASCII coded.

Values	Function
48	"0" - (low) bit is always 0
49	"1" - (high) bit is always 1
69	"E" - (even) even parity (default)
78	"N" - (no) no bit
79	"O" - (odd) odd parity

Receive timeout

This register is used to set the duration until a receive timeout is triggered.

The message is considered to be terminated when nothing is transfered for the specified duration.
The time is specified here in characters to ensure that it is independent of the transfer rate. The number of characters is then multiplied by the time needed to transfer a character.

Values	Function
0	Function disabled
1 to 65,535	Receive timeout in characters (default = 4)

Transmit timeout

This register is used to set the duration until a transmit timeout is triggered.

The message is considered to be terminated when nothing is transfered for the specified duration.
The time is specified here in characters to ensure that it is independent of the transfer rate. The number of characters is then multiplied by the time needed to transfer a character.

Values	Function
0	Function disabled
1 to 65,535	Transmit timeout in characters (default = 5)

FlatStream mode

In the input direction, the transmit array is generated automatically. This register offers two options to the user that allow an incoming data stream to have a more compact arrangement. Once enabled, the program code for evaluation must be adapted accordingly.

Information:

All B&R modules that offer FlatStream mode support the options "Large segments" and "MultiSegmentMTUs" in the output direction. Compact transmission only needs to be explicitly allowed in the input direction.

Bit	Name	Value	Information
0	MultiSegmentMTU	0	Not allowed (default)
		1	Allowed
1	Large segments	0	Not allowed (default)
		1	Allowed
2 - 7	Reserved	-	

Standard

By default, both options relating to compact transmission in the input direction are disabled.

1. The module only forms segments that are at least one byte smaller than the enabled MTU. Each sequence begins with a control byte so that the data stream is clearly structured and relatively easy to evaluate.
2. Since a FlatStream message can be of any length, the last segment of the message frequently doesn't fill up all of the MTU's space. By default, the remaining bytes during this type of transfer cycle are not used.

MultiSegmentMTUs allowed

With this option, the InputMTU is completely filled (if enough data is pending). The previously unfilled Rx bytes transmit the next control bytes and their segments. This allows the enabled Rx bytes to be used more efficiently.

Large segments allowed:

When transmitting very long messages or when enabling only very few Rx bytes, then a great many segments must be created by default. The bus system is more stressed than necessary since an additional control byte needs to be created and transmitted for each segment. With the "Large segments" option, the segment length is limited to 63 bytes independently of the InputMTU. One segment can stretch across several sequences, i.e. it is possible for "pure" sequences to occur without a control byte.

Information:

It is still possible to split up a message into several segments, however. If this option is used and messages with more than 63 bytes occur, for example, then messages can still be split up among several segments.

Using both options

It is also possible to use both options at the same time.

7.3.9.4 X20CS1070

Register	Name	Bytes	Module X20CS1070-C01	
Input:				
0	Input sequence	1	Byte	
1	RxByte 1	1	Byte	
2	RxByte 2	1	Byte	
3	RxByte 3	1	Byte	
4	RxByte 4	1	Byte	
5	RxByte 5	1	Byte	
6	RxByte 6	1	Byte	
7	RxByte 7	1	Byte	
Output:				
32	Output sequence	1		Byte
33	TxByte 1	1		Byte
34	TxByte 2	1		Byte
35	TxByte 3	1		Byte
36	TxByte 4	1		Byte
37	TxByte 5	1		Byte
38	TxByte 6	1		Byte
39	TxByte 7	1		Byte
197	Flatstream mode	1		2)
199	Number of unacknowledged sequences	1		2)
257	Baud rate	1		2)
259	Synchronization Jump Width	1		2)
261	Offset of the sampling instant	1		2)
266	Number of CAN objects	2		2)
Data bytes in DP frame			8 in	8 out

2) The register can be modified in the parameter dialog box for the I/O module and is transferred acyclically.

Support with firmware version ≥ V1.43

Input sequence

This register contains information about the communication status of the module. It is written by the module and should only be read by the CPU.

Bit	Name	Value	Information
0 - 2	Input sequence counter	0 to 7	Counter for sequences issued in the input direction
3	InputSynchronous	0	Not ready (disabled)
		1	Ready (enabled)
4 - 6	Acknowledged output sequence	0 to 7	Mirrors the output sequence counter value
7	OutputSynchronous	0	Not ready (disabled)
		1	Ready (enabled)

Input sequence counter

The input sequence counter is a continuous counter of sequences that have been issued by the module. The module uses the input sequence counter to direct the CPU to accept a sequence (the input direction must be synchronized when this happens).

InputSynchronous

The module uses this to attempt to synchronize the input channel.

Acknowledged output sequence

This value is used for acknowledgment. The value of the output sequence counter is mirrored if the module has received a sequence successfully.

OutputSynchronous

This bit acknowledges the synchronization of the output channel for the CPU. This indicates that the module is ready to receive data.

RxByte

The Tx and Rx bytes are cyclic registers used to transport the payload data and the necessary control bytes.
In the user program, only the Tx and Rx bytes from the CPU can be used. The corresponding counterparts are located in the module and are not accessible to the user. For this reason, names were chosen from the CPU point of view.

- "T" - "Transmit" →CPU *transmits* data to the module.
- "R" - "Receive" →CPU *receives* data from the module.

Values
0 to 65,535

Output sequence

This register contains information about the communication status of the CPU. It is written by the CPU and read by the module.

Bit	Name	Value	Information
0 - 2	Output sequence counter	0 to 7	Counter for sequences issued in the output direction
3	OutputSynchronous	0	Output direction disabled
		1	Output direction enabled
4 - 6	Acknowledged input sequence	0 to 7	Mirrors the input sequence counter value
7	InputSynchronous	0	Input direction not ready (disabled)
		1	Input direction ready (enabled)

Output sequence counter

The output sequence counter is a continuous counter of sequences that have been issued by the CPU. The CPU uses the output sequence counter to direct the module to accept a sequence (the output direction must be synchronized when this happens).

OutputSynchronous

The CPU uses this bit to attempt to synchronize the output channel.

Acknowledged input sequence

This value is used for acknowledgment. The value of the input sequence counter is mirrored if the CPU has received a sequence successfully.

InputSynchronous

This bit acknowledges the synchronization of the input channel for the module. This indicates that the CPU is ready to receive data.

TxByte

See RxByte

Flatstream mode

In the input direction, the transmit array is generated automatically. This register offers two options to the user that allow an incoming data stream to have a more compact arrangement. Once enabled, the program code for evaluation must be adapted accordingly.

Information:

All B&R modules that offer FlatStream mode support the options "Large segments" and "MultiSegmentMTUs" in the output direction. Compact transmission only needs to be explicitly allowed in the input direction.

Bit	Name	Value	Information
0	MultiSegmentMTU	0	Not allowed (default)
		1	Allowed
1	Large segments	0	Not allowed (default)
		1	Allowed
2 - 7	Reserved	-	

Standard

By default, both options relating to compact transmission in the input direction are disabled.

1. The module only forms segments that are at least one byte smaller than the enabled MTU. Each sequence begins with a control byte so that the data stream is clearly structured and relatively easy to evaluate.
2. Since a FlatStream message can be of any length, the last segment of the message frequently doesn't fill up all of the MTU's space. By default, the remaining bytes during this type of transfer cycle are not used.

MultiSegmentMTUs allowed

With this option, the InputMTU is completely filled (if enough data is pending). The previously unfilled Rx bytes transmit the next control bytes and their segments. This allows the enabled Rx bytes to be used more efficiently.

Large segments allowed:

When transmitting very long messages or when enabling only very few Rx bytes, then a great many segments must be created by default. The bus system is more stressed than necessary since an additional control byte needs to be created and transmitted for each segment. With the "Large segments" option, the segment length is limited to 63 bytes independently of the InputMTU. One segment can stretch across several sequences, i.e. it is possible for "pure" sequences to occur without a control byte.

Information:

It is still possible to split up a message into several segments, however. If this option is used and messages with more than 63 bytes occur, for example, then messages can still be split up among several segments.

Using both options

It is also possible to use both options at the same time.

Number of unacknowledged sequences

With this register, the user specifies how many unacknowledged sequences the module is allowed to transmit.

Recommendation:
X2X Link: Max. 5
POWERLINK: Max. 7

Values	Infomation
1 to 7	Default: 1

Baud rate

Configuration of the CAN transfer rate for the interface.

Bit	Description	Value	Information
0 - 3	Transfer rate	1	10 kbit/s
		2	20 kbit/s
		3	50 kbit/s
		4	100 kbit/s
		5	125 kbit/s
		6	250 kbit/s
		7	500 kbit/s (default)
		8	800 kbit/s
		9	1000 kbit/s
4 - 7	Reserved	-	

Synchronization Jump Width

The synchronization jump width is used to resynchronize the sample point within a CAN telegram.

A detailed description of the synchronization jump width can be found in the CAN specification.

Values	Function
0 to 4	Synchronization jump width (default = 3)

Offset of the sampling instant

Offset for the sample instant of the individual bits on the CAN bus.

A detailed description of the sampling instant can be found in the CAN specification.

Values	Function
0 to 1	Sampling instant offset (default = 0)

Number of CAN objects

Defines the number of CAN objects that must be copied to the transmit buffer before the transmission is started.

Values	Function
0 to 8	Number of CAN objects in the transmit buffer before transmission is started (default = 1)

7.3.10 Motor modules

7.3.10.1 X20MM2436

Register	Name	Bytes	Module	
			X20MM2436-C02	
Input:				
0	Counter 1	2	Word	
2	Counter 2	2	Word	
10	**HI:** 0 **LO:** Input status	2	Word	
32	**HI:** 0 **LO:** Error status	2	Word	
Output:				
12	PWM period duration	2		Word
14	PWM pulse width or current 1	2		Word
16	PWM pulse width or current 2	2		Word
18	Dither amplitude	1		1)
20	Dither frequency	1		1)
30	Module configuration	1		1)
34	**HI:** 0 **LO:** Error acknowledgment / dither switch-off	2		Word
Data bytes in DP frame			8 in	8 out

1) The register can be modified in the parameter dialog box for the I/O module and is transferred acyclically.

Counter

This register indicates the status of counters 1 and 2.

Values
-32,768 to 32,767

Input status

The status of the inputs and counters is mapped in this register.

This function is available beginning with firmware Version 4.

Bit	Description	Value	Information
0	Input status	0 or 1	Logical state of input 1
...		...	
3	Input status	0 or 1	Logical state of input 4
4	Counter overflow 1	0	Period duration or gate measurements of counter 1 are within the valid range (0x0 - 0xFFFF). The bit is only valid if overflow detection is enabled (bit 2 = 1 in the Error acknowledgment / dither switch-off register).
		1	Overflow during period duration or gate measurement (reset with bit 2 = 0 in the Error acknowledgment / dither switch-off register).
5	Counter overflow 2	0	Period duration or gate measurements of counter 2 are within the valid range (0x0 - 0xFFFF). The bit is only valid if overflow detection is enabled (bit 3 = 1 in the Error acknowledgment / dither switch-off register).
		1	Overflow during period duration or gate measurement (reset with bit 3 = 0 in the Error acknowledgment / dither switch-off register).
6	Reference toggle	x	Bit 6 changes value each time the counter state is latched from counter 1 to counter 2. After the module boots, bit 6 = 0.
7	Reserved	-	

Error status

If an error is detected, the corresponding error bit in this register remains set until the error is acknowledged in the Error acknowledgment / dither switch-off register.

Bit	Description	Value	Information
0	Undervoltage	0	No error
		1	Module supply lower limit <18 V
1	Overvoltage	0	No error
		1	Module supply upper limit >50 V
2	Overtemperature	0	No error
		1	Overtemperature
3	Reserved	-	
4	Current error - channel 1	0	No error
		1	Open load - output 1
5	Open load - channel 1	0	No error
		1	Overcurrent - output 1
6	Open load - channel 2	0	No error
		1	Open load - output 2
7	Overcurrent - channel 2	0	No error
		1	Overcurrent - output 2

An overcurrent error is registered if one of the following conditions is met:

- ≥3.5 A flow from a PWM output for at least 2 seconds
- ≥5 A flow for 3 consecutive PWM cycles

In both cases, the affected PWM output is deactivated by the firmware (i.e. the pins on the PWM output are short-circuited). The user must acknowledge the error before a PWM output disabled in this manner can be made operational again.

An open load error is only registered in current control mode (see Module configuration) if the current setpoint is not reached. In some cases this can be caused by an open line, although usually the impedance of the load is too high.

PWM period duration

This register can be used to set the period duration between 20 µs (50 kHz) and 65,535 µs (15 Hz).

Values	Information
20 to 65535	Time in µs

PWM pulse width or current

The PWM pulse width (PWM mode) or current setting (in current mode) is entered in this register according to the setting in the module configuration register. A negative value changes the output polarity.

Information:

This module uses the same scaling as the X67MM2436 module to maintain software compatibility. Current values larger than 3.5 A are limited to 3.5 A.

Derating must also be taken into consideration when using both channels.

PWM mode

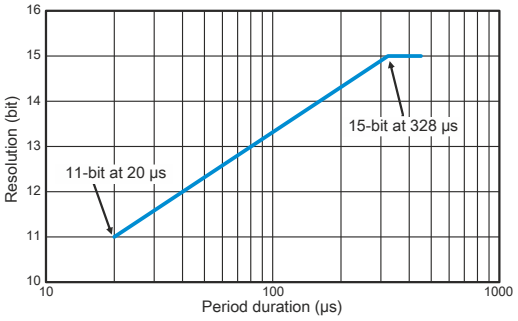
Values	Output +	Output -
32767	high	Low
16384	PWM 50/50	Low
0	Low	Low
-16384	Low	PWM 50/50
-32767	Low	high

Current mode

Values	Current mode	Note
22937 to 32767	+3.5 A (max. 2 s)	Limited internally, check derating
22936	3.5 A (max. 2 s)	Derating must be taken into consideration.
19660	+3 A	
0	0 A	
-19660	-3 A	
-22936	-3.5 A (max. 2 s)	Derating must be taken into consideration.
-22937 to -32767	-3.5 A (max. 2 s)	Limited internally, check derating

Resolution/Derating

As mentioned earlier in the technical data, the PWM resolution is 15-bit (+ sign). This value is derated for a period duration of less than 328 µs because of the minimal PWM timing resolution (10 ns) (see following diagram). With the minimum PWM period duration of 20 µs, the PWM has 11-bit resolution (+ sign):



Dither amplitude

This register can be used to configure the amplitude value or pulse width.
0 to 255 corresponds with an amplitude value from 0.0 to 25.5% of the maximum current or the maximum pulse width of 32,767.

Values	Information
0 to 255	Amplitude value or pulse width

Dither frequency

This register can be used to set the frequency in 2 Hz steps.

Values	Information
0 to 255	Corresponds to 0 to 510 Hz

Module configuration

The output control for each motor can be configured separately in this register.

Bit	Description	Value	Information
0	Output 1	0	PWM control
		1	Current control
1	Output 2	0	PWM control
		1	Current control
2 - 7	Reserved	-	

Error acknowledgment / dither switch-off

This register can be used to acknowledge errors or to enable/disable overflow detection, counters and dither.

This function is available beginning with firmware Version 4.

Bit	Description	Value	Information
0	Acknowledge error 1	0	No effect
		1	Error acknowledgment on output 1 (overcurrent or open load) or acknowledgment from limit switch 1
1	Acknowledge error 2	0	No effect
		1	Error acknowledgment on output 2 (overcurrent or open load) or acknowledgment from limit switch 2
2	Overflow detection 1	0	Overflow detection disabled. Bit 4 in the counter status register is reset (see section Input status)
		1	Counter 1: Overflow detection enabled.
3	Overflow detection 2	0	Overflow detection disabled. Bit 5 in the counter status register is reset (see section Input status)
		1	Counter 2: Overflow detection enabled.
4	Counter 1	0	Counter 1 is enabled (default).
		1	Counter 1 is set to 0 and disabled.
5	Counter 2	0	Counter 2 is enabled (default).
		1	Counter 2 is set to 0 and disabled (no effects if counter 1 is configured as an ABR counter)
6	Dither 1	0	Dither for PWM output 1 is enabled (default). The dither frequency and dither amplitude must be >0.
		1	Dither for PWM output 1 is disabled.
7	Dither 2	0	Dither for PWM output 2 is enabled (default). The dither frequency and dither amplitude must be >0.
		1	Dither for PWM output 2 is disabled.

7.3.10.2 X20MM4456

Register	Name	Bytes	Module X20MM4456-C02	
Input:				
0	ABR counter 1	2	Word	
2	ABR counter latch 1	2	Word	
4	µs since trigger 1	2	Word	
6	Input status 1	1	Byte	
7	Global error messages	1	Byte	
8	ABR counter 2	2	Word	
10	ABR counter latch 2	2	Word	
12	µs since trigger 2	2	Word	
14	Input status 2	1	Byte	
15	Channel errors	1	Byte	
16	ABR counter 3	2	Word	
18	ABR counter latch 3	2	Word	
20	µs since trigger 3	2	Word	
22	Input status 3	1	Byte	
24	ABR counter 4	2	Word	
26	ABR counter latch 4	2	Word	
28	µs since trigger 4	2	Word	
30	Input status 4	1	Byte	
Output:				
0	PWM pulse width or current 1	2		Word
2	Control 1	1		Byte
4	PWM period duration	2		Word
8	PWM pulse width or current 2	2		Word
10	Control 2	1		Byte
16	PWM pulse width or current 3	2		Word
18	Control 3	1		Byte
24	PWM pulse width or current 4	2		Word
26	Control 4	1		Byte
197	Dither amplitude	1		2)
199	Dither frequency	1		2)
257	Engine configuration 1	1		2)
259	Engine configuration 2	1		2)
261	Engine configuration 3	1		2)
266	Engine configuration 4	1		2)
	Data bytes in DP frame		30 in	14 out

2) The register can be modified in the parameter dialog box for the I/O module and is transferred acyclically.

Support with firmware version ≥ V1.43

ABR counter

These registers are 16-bit AB(R) counters.

Values
-32,768 to 32,767

ABR counter latch

When a latch event occurs, the current counter values are saved in these registers. For additional features, see bit 5 in the respective Control register.

Values
-32,768 to 32,767

µs since trigger

This register shows either the time in µs since the last trigger event or the average current value.

- The "µs Since Trigger" counter cannot overrun, i.e. the counter is stopped at 2^{16}-1 and retains this value until the next time the trigger function is activated
- If the average current is displayed in this register (bit 11 in the respective Engine configuration register), then the data type of µs Since Trigger in Automation Studio must be unsigned integer (UINT). The average current value, on the other hand, is an Integer (INT). This means that negative currents are displayed between 32769 and 65535.

Counting mode

Values
0 to 65535

Measurement of average current value

Values	Information
19661 to 32767	6 to 10 A
19660	6 A
1	305 µA (= 10 A / 32,767)
0	0 A
65535	-305 µA (= -10 A / 32,767)
45876	-6 A
45875 to 32769	-6 to -10 A

Input status

These registers indicate the status of the inputs and outputs for each DC motor.

The following placeholders are used in the status table.

Register	[x]	In1	In2	In3	In4
Status of inputs 1	1	DI1	DI2	DI3	DI4
Status of inputs 2	2	DI5	DI6	DI7	DI8
Status of inputs 3	3	DI9	DI10	DI11	DI12
Status of inputs 4	4	DI13	DI14	DI15	DI16

Bit	Description	Value	Information
0	StatusInput **[In1]**	x	**Ein1** is used for the encoder signal A of ABR counter **[x]**.
1	StatusInput **[In2]**	x	**Ein2** is used for the encoder signal B of ABR counter **[x]**.
2	StatusInput [**In3]**	0	Possible uses for the digital input • Trigger input **[x]** • Reference pulse for ABR counter **[x]** • Limit switch **[x]** (left)
3	StatusInput **[In4]**	0	Possible uses for the digital input • Reference enable **[x]** • Trigger input **[x]** • Limit switch **[x]** (right)
4	nLatchPending **[x]**	00	Latching started
		01	ABR counter latch **[x]** ready. Latch not yet started.
5	LatchDone **[x]**	0	The status of this bit is changed each time ABR counter **[x]** is successfully latched
6	EndswitchReached **[x]**	00	No effect on PWM output **[x]**
		01	Limit switch **[x]** reached. PWM output **[x]** disabled.
7	PWMError **[x]**	0	Error free operation
		1	An error has occurred. The error can be determined by evaluating the two error registers Global error messages and Channel errors.
8 - 15	Status of inputs 1	x	With "Status of inputs 1", bits 12 to 15 contain error bits 4 to 7 from the register Global error messages
	Status of inputs 2	x	With "Status of inputs 2", bits 8 to 15 contain error bits 0 to 7 from the register Channel errors

Global error messages

This register indicates overtemperature and errors in the module supply. The error bits are automatically acknowledged by the module as soon as the values are back within the permissible limits.

Bit	Description	Value	Information
0 - 3	Reserved	0	
4	Overvoltage	0	No error
		1	Voltage >80 V. All outputs are deactivated.
5	Undervoltage	0	No error
		1	Voltage <18 V
6	Voltage warning	0	No error
		1	Voltage >60 V
7	Overtemperature	0	No error
		1	Module overtemperature; all outputs are deactivated.

Channel errors

If an error is detected, the corresponding error bit in this register remains set until the error is acknowledged using bit 4 in the respective Control register.

Bit	Description	Value	Information
0	Open load error 1	0	No error
		1	Open load error
1	Overcurrent error 1	0	No error
		1	Overcurrent error. The output is disabled.
2	Open load error 2	0	No error
		1	Open load error
3	Overcurrent error 2	0	No error
		1	Overcurrent error. The output is disabled.
4	Open load error 3	0	No error
		1	Open load error
5	Overcurrent error 3	0	No error
		1	Overcurrent error. The output is disabled.
6	Open load error 4	0	No error
		1	Open load error
7	Overcurrent error 4	0	No error
		1	Overcurrent error. The output is disabled.

Overcurrent error

An overcurrent error is registered if one of the following conditions is met:

- ≥10 A flow from a PWM output for at least 2 seconds
- ≥16 A flow for 3 consecutive PWM cycles
- All PWM outputs together consume more than 32 A on the X3 connector

In all three cases, the affected PWM output is disabled by the firmware (i.e. the pins on the PWM output are short-circuited). The user must acknowledge the error using bit 4 in the respective Control register before a PWM output disabled in this manner can be made operational again.

Open load error

An open load error is only registered in current control mode (see bit 12 in the respective Engine configuration register) if the set current is not reached. In some cases this can be caused by an open circuit, although usually the impedance of the load is too high.

PWM pulse width or current

The PWM pulse width (PWM mode) or current setting (in current mode) is entered in this register according to the setting in the module configuration register. A negative value changes the output polarity.

PWM mode

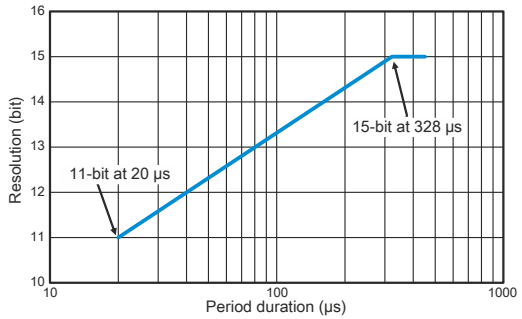
Values	Output +	Output -
32767	high	Low
16384	PWM 50/50	Low
0	Low	Low
-16384	Low	PWM 50/50
-32767	Low	high

Current mode

Values	Current mode
19661 to 32767	6 to 10 A (max. 2 s)
19660	6 A
0	0 A
-19660	-6 A
-19661 to -32767	-6 to -10 A (max. 2 s)

Resolution/Derating

As mentioned earlier in the technical data, the PWM resolution is 15-bit (+ sign). This value is derated for a period duration of less than 328 µs because of the minimal PWM timing resolution (10 ns) (see following diagram). With the minimum PWM period duration of 20 µs, the PWM has 11-bit resolution (+ sign):



Control

These registers can be used to configure the behavior of the trigger, the ABR counter and the dither.

[x] represents the corresponding control number.

Bit	Description	Value	Information
0	Configuration of trigger edge for µs Since Trigger	0	Counting starts at rising edge
		1	Counting starts at falling edge
1	Status change of bit 1 enables µs Since Trigger	x	Counting starts at the next trigger edge (see bit 0). For more information about trigger functionality, see "Trigger function procedure".
2	Latching and referencing ABR counter	0	Disabled
		1	Enabled
3	Dither	0	Dither for PWM output **[x]** is enabled (default setting). The dither frequency and dither amplitude must be >0.
		1	Dither for PWM output **[x]** is disabled.
4	Acknowledge error or limit switch	0	No effect
		1	Error acknowledgment on output **[x]** (overcurrent or open load) or acknowledgment from limit switch **[x]**
5	Configuration of registers ABR counter latch and µs since trigger	0	The register ABR counter latch **[x]** contains the latched counter value. The register µs since trigger**[x]** contains the trigger counter.
		1	Both registers contain the current PWM output current
6	Reset ABR counter	0	Enable ABR counter (default)
		1	Reset ABR counter
7	Reserved	0	

Trigger function procedure

The following points must be taken into consideration when configuring or activating the trigger function:

- Select the desired trigger edge using bit 0
- Enable the trigger function by changing the state of StartTrigger (bit 1). This edge clears the register µs since trigger (µs counter).
- When the trigger event occurs, the µs counter "µs Since Trigger" is started
- The "µs Since Trigger" counter cannot overrun, i.e. the counter is stopped at 2^{16}-1 and retains this value until the next time the trigger function is activated
- The trigger function can be re-activated at any time by changing the state of StartTrigger (bit 1) regardless of if a trigger event has occurred or if "µs Since Trigger" has reached its maximum value.

Reset ABR counter

Bit 6 sets the following counters and status bits to 0:

- ABR counter
- Latch value of the ABR counter
- Latching started on the ABR counter (bit 4 of Input status)
- ABR counter successfully latched (bit 5 of Input status)

Please note that a started latch procedure is no longer active after the ABR counter has been reset. This means that latching must be restarted by a rising edge on bit 2.

PWM period duration

This register can be used to set the period duration between 20 µs (50 kHz) and 65,535 µs (15 Hz).

Values	Information
20 to 65535	Time in µs

Dither amplitude

This register can be used to configure the amplitude value or pulse width.
0 to 255 corresponds with an amplitude value from 0.0 to 25.5% of the maximum current or the maximum pulse width of 32,767.

Values	Information
0 to 255	Amplitude value or pulse width

Dither frequency

This register can be used to set the frequency in 2 Hz steps.

Values	Information
0 to 255	corresponds to 0 to 510 Hz.

Engine configuration

These registers can be used to configure the four DC motors.

The following placeholders are used in the configuration table:

[x]	In1	In2
1	DI3	DI4
2	DI7	DI8
3	DI11	DI12
4	DI15	DI16

Bit	Description	Value	Information
0 - 1	Configuration of the latch function for the ABR counter. Activation of the latch function is described in the control register (bit 2)	00	ABR counter **[x]** is latched unconditionally (default setting). The reference enable input is ignored.
		01	ABR counter **[x]** is latched if a rising edge occurs on digital input **Ein1** and the reference enable input **Ein2** is "1". The reference enable input must be activated to do this (see bit 2).
		10	ABR counter 1 is latched if a rising edge occurs on digital input **Ein1** and the reference enable input **Ein2** is "1". The reference enable input must be activated to do this (see bit 2).
		11	The latch function is disabled.
2	Reference for enable input	0	No reference enable input
		1	Digital input **Ein2** is used as a reference enable input
3	Active level of the reference enable for the ABR counter	0	Active level = High
		1	Active level = Low
4 - 5	Reserved	0	
6 - 7	Definition of the limit switch (see also Limit switch function)	00	Limit switch 1 is disabled
		01	Digital input **In1** is used as the limit switch
		10	Digital input **In2** is used as the limit switch
		11	Digital inputs **In1** and **In2** are used as left and right limit switches
8	Active level for limit switch	0	Active level = High
		1	Active level = Low
9 - 10	Trigger input for trigger counter "µs Since Trigger"	00	Trigger counter disabled
		01	Digital input **In1** is used as trigger input
		10	Digital input **In2** is used as trigger input
		11	Reserved
11	Displays the current average for the output	0	If the corresponding setting has been enabled, then the average current value is indicated in register ABR counter latch**[x]** (see bit 5 in register Control)
		1	If the corresponding setting has been enabled, then the average current value is indicated in register µs since trigger**[x]** (see bit 5 in register Control)
12	Type of control for the output	0	PWM control
		1	Current control
13 - 14	PWM decay configuration	00	Slow decay (default setting)
		01	Mixed decay
		10 to 11	Reserved
15	Reserved	0	

Limit switch function

The limit switch function serves to quickly shut off the PWM outputs when a limit position is reached.

The limit switch is activated and the disable edge (rising or falling) on the limit switch input is selected using bits 6 to 8.

A PWM output is disabled as soon as the configured disable edge is reached on the corresponding input of the limit switch. It remains disabled until either the limit switch function is disabled or the limit switch is acknowledged with bit 4 in the corresponding Control register.

7.3.10.3 X20SM14x6

Register	Name	Bytes	Module			
			X20SM1426*1) X20SM1426-C10 X20SM1436*1) X20SM1436-C10		X20SM1426-C05 X20SM1436-C05	
Input:						
0	Current position 1	4	Long		Long	
4	Status 1	2	Word		Word	
6	**HI:** 0 **LO:** Digital inputs	2	Word		Word	
Output:						
0	Position/speed 1	4		Long		Long
4	Control 1	2		Word		Word
6	**HI:** 0 **LO:**Mode 1	2		Word		Word
Data bytes in DP frame			8 in	8 out	8 in	8 out

1) The configuration registers (see "Ramp model" section in module description) can be modified in the parameter dialog box for the I/O module and are transferred asynchronously.

Module names with '*': Support with firmware version ≥ V1.43

Current position

This cyclic register contains the current position.

Default: Value of the internal position counter, can be changed to ABR counter

Values
-2,147,483,648 to 2,147,483,647

Status

The bits in this register reflect the state of the state machine.

Bit	Description	Value	Information
0	Ready to switch on	x	
1	Switched on	x	
2	Operation enabled	x	
3	Fault (error bit)	x	
4	Voltage enabled	x	
5	Quick stop	x	
6	Switch on disabled	x	
7	Warning	x	
8	Reserved	0	
9	Remote	1	Always 1 because there is no local mode for the SM module
10	Target reached	x	
11	Internal limit active	0	No limit violation
		1	Internal limit is active (upper/lower software limit violated)
12	Mode-specific	x	
13 - 15	Reserved	0	

Digital inputs

This register indicates the logical states of digital inputs.

Bit	Description	Value	Information
0	Digital input 1	0 or 1	Input state - Digital input 1
...		...	
3	Digital input 4	0 or 1	Input state - Digital input 4
4 - 15	Reserved	0	

Position/speed

This register is used to set position or speed, depending on the operating mode.

- Position mode (see Mode): Cyclic setting of the position setpoint in microsteps. In this mode, one micro-step is always 1/256 full-step.
- Speed mode (see Mode): In this mode, this register is considered a signed speed setpoint.

Values
-2,147,483,648 to 2,147,483,647

Control

This register can be used to issue commands based on the module's state.

Bit	Description	Value	Information
0	Switch on	x	
1	Enable voltage	x	
2	Quick stop	x	
3	Enable operation	x	
4 - 6	Mode-specific	x	
7	Fault reset	x	
8	Halt[1)]	x	
9 - 10	Reserved	0	
11	Motor ID trigger	0	No effect
		1	Rising edge: Motor ID trigger[2)]
12	Warning reset	0	No effect
		1	Rising edge: Reset warnings
13	Undercurrent detection	0	Disable current error detection (default)
		1	Enable current error detection
14	ABR counter sync/async	0	Default: • Internal position counter, cyclic • ABR counter, acyclic
		1	• Internal position counter, acyclic • ABR counter, cyclic
15	Stall detection	0	Disable stall detection (default)
		1	Enable stall detection

1) The "Halt" bit is only evaluated when the extended control word is enabled.
2) This bit can be used to trigger a measurement of the motor ID. Keep in mind that the application must ensure that the conditions are fulfilled for this.

Mode

Values	Information
0	No mode selected
1	The position setpoint is specified as set in the Position/speed register. The motor is then moved to this new position. This is done with a ramp function that accounts for the defined maximum speed and acceleration values. The position setpoint can also be changed during an active positioning procedure. The position setpoint is specified in microsteps (1/256 of a full step). The position setpoint will be applied as soon as it differs from the current position. Then the new position is used for the movement.
2	The value in the Position/speedregister is interpreted as the speed setpoint (microsteps/cycle). Observing the maximum permissible acceleration, the motor moves with a ramp to the desired speed setpoint and maintains this speed until a new speed setpoint is specified. Values are allowed within the range -65535 to 65535. When a value is entered outside of this range, it is readjusted to these limits.

Information:

For all modes: The "Target reached" bit is set in the Status register when the current action is finished (i.e. when the position or speed is reached, depending on the mode).

A new position or speed can be specified even before the current action is finished.

7.3.11 Other modules

7.3.11.1 X20CM8281

Register	Name	Bytes	Module			
			X20CM8281-C01		X20CM8281-C03	
Input:						
0	**HI:** Reserved **LO:** Digital inputs and ouput status 1 - 4	2	Word		Word	
4	Counter 1	2	Word		Word	
6	Counter 2	2	Word		Word	
8	Analog input	2	Word		Word	
16	**HI:** Reserved **LO:** Input latch	2	Word		Word	
31	**HI:** Reserved **LO:** Analog input status[1)]	2	Word		Word	
Output:						
2	**HI:** Reserved **LO:** Digital outputs 1 - 2	2		Word		Word
10	Analog output	2		Word		Word
12	Digital input filter	1		[2)]		[2)]
18	**HI:** Reserved **LO:** Reset input latch	2		Word		Word
14	**HI:** Reserved **LO:** Counter configuration	2		[2)]		Word
22	Analog input filter	1		[2)]		[2)]
24	Configuring analog input channels	1		[2)]		[2)]
Data bytes in DP frame			12 in	6 out	12 in	8 out

1) Diagnostics information is automatically sent to the PROFIBUS DP master.
2) The register can be modified in the parameter dialog box for the I/O module and is transferred acyclically.

Digital inputs and ouput status

This register is used to indicate the input state of the digital inputs and the status of the digital outputs.

Bit	Name	Value	Information
0	Input channel 1	0 or 1	Input state - Digital input 1
...		...	
3	Input channel 4	0 or 1	Input state - Digital input 1
4	Status output 1	0	Digital output channel 1: No error
		1	Digital output channel 1: Short circuit or overload
5	Status output 2	0	Digital output channel 1: No error
		1	Digital output channel 1: Short circuit or overload
6 - 7	Reserved	-	

Counter

Counter 1 is intended for event counter operation.

It is possible to switch between event counter operation or gate measurement for Counter 2.

Values
0 to 65,535

Analog input

The analog input value is mapped in this register depending on the configured operating mode.

Values	Input signal:
-32,768 to 32,767	Voltage signal -10 to 10 VDC
0 to 32,767	Current signal 0 to 20 mA
0 to 32,767	Current signal 4 mA to 20 mA

Input latch

This register is used to indicate input state of digital inputs 1 to 4 after expiration of the input filter time.

Bit	Name	Value	Information
0	Latch channel 1	0 or 1	Input state of digital input 1 after expiration of the delay time
...		...	
3	Latch channel 4	0 or 1	Input state of digital input 4 after expiration of the delay time
4 - 7	Reserved	-	

Analog input status

This register is used to monitor the analog input on the module. A change in the monitoring status generates an error message.

Bit	Description	Value	Information
0 - 1	Channel 1	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line[1)]
2 - 7	Reserved	0	

1) Open-circuit detection does not occur during current signal measurement.

Digital outputs

This register is used to store the switching state of digital outputs 1 to 2.

Bit	Name	Value	Information
0	Channel 1	0	Digital output 01 reset
		1	Digital output 01 set
1	Channel 2	0	Digital output 02 reset
		1	Digital output 02 set

Analog output

This register is used to output the analog output value appears depending on the operating mode that is set.

Values	Information
-32,768 to 32,767	Voltage signal -10 to 10 VDC
0 to 32,767	Current signal 0 to 20 mA

Digital input filter

This register can be used to specify the filter value for all digital inputs.

The filter value can be configured in steps of 100 µs. It makes sense to enter values in steps of 2, however, since the input signals are sampled every 200 µs.

Values	Filter
0	No software filter
2	0.2 ms
...	...
250	25 ms - Higher values are limited to this value

Reset input latch

This register is used to reset the input latches channel by channel.

Bit	Name	Value	Information
0	Channel 1	0	No influence on the latch status
		1	Resets the latch status
...		...	
3	Channel 4	0	No influence on the latch status
		1	Resets the latch status
4 - 7	Reserved	-	

Counter configuration

This register can be used to configure and reset the individual counters.

Bit	Name	Value	Information
0 - 3	Counter 2 (counter frequency, only with gate measurement)	0	48 MHz
		1	3 MHz
		2	187.5 kHz
		3	24 MHz
		4	12 MHz
		5	6 MHz
		6	1.5 MHz
		7	750 kHz
		8	375 kHz
4	Reset counter 1	0	No influence on the counter
		1	Clear counter (at rising edge)
5	Reset counter 2	0	No influence on the counter
		1	Clear counter (at rising edge)
6 - 7	Counter 2 (operating mode)	0	Event counter measurement
		1	Gate measurement

This register also includes configuration data in addition to the cyclic data. If the register is used cyclically and in the init script, then the preset configuration only remains available when operated directly on the CPU. On the bus controller, the configuration is always overwritten with 0.

However, starting with upgrade version 1.0.2.1, the cyclic bit can be hidden in order to prevent the configuration from being overwritten.

Information:

If the counter should be cleared, this must be done using an acyclic write command. When doing so, the configuration bit must be transferred together with the reset counter bit!

Analog input filter

This register is used to define the filter level and input ramp limitation of the input filter.

Bit	Description	Value	Information
0 - 2	Defines the filter level	000	Filter switched off
		001	Filter level 2
		010	Filter level 4
		011	Filter level 8
		100	Filter level 16
		101	Filter level 32
		110	Filter level 64
		111	Filter level 128
3	Reserved	0	
4 - 6	Defines the input ramp limitation	000	The input value is used without limitation
		001	Limit value = 0x3FFF (16383)
		010	Limit value = 0x1FFF (8191)
		011	Limit value = 0x0FFF (4095)
		100	Limit value = 0x07FF (2047)
		101	Limit value = 0x03FF (1023)
		110	Limit value = 0x01FF (511)
		111	Limit value = 0x00FF (255)
7	Reserved	0	

Configuring analog input channels

This register can be used to define the type and range of signal measurement.

Each channel is capable of handling either current or voltage signals. The type of signal is determined by the connection terminals used. Since current and voltage require different adjustment values, it is also necessary to configure the desired type of output signal.

Bit	Description	Value	Information
0 - 1	Analog input	00	Voltage signal -10 VDC to +10 VDC
		01	Current signal 0 mA to 20 mA
		11	Current signal 4 mA to 20 mA
2 - 3	Reserved	0	
4	Analog output	0	Voltage signal -10 VDC to +10 VDC
		1	Current signal 0 mA to 20 mA
5 - 7	Reserved	0	

7.3.11.2 X20CMRx1x

Register	Description	Bytes	Module			
			X20CMR010		X20(c)CMR011 X20CMR111	
Input:						
2	Relative humidity	2	Word		Word	
6	Temperature	2	Word		Word	
10	Acceleration 1	2			Word	
14	Acceleration 2	2			Word	
18	Acceleration 3	2			Word	
22	Rotation 1	2			Word	
26	Rotation 2	2			Word	
30	Rotation 3	2			Word	
34	Analog inputs 1	2			Word	
38	Analog inputs 2	2			Word	
41	**HI:** Reserved **LO:** Status input/output and I/O power supply	2			Word	
46	Module status	2			Word	
Output:						
129	Switching state of the digital output	1				Byte
Data bytes in DP frame			4 in	0 out	24 in	1 out

Relative humidity

An internal sensor measures the relative humidity in the area.

Values	Information
0 to 100	Relative humidity [%], resolution 1%

Temperature

An internal sensor measures the ambient temperature.

Values	Information
-250 to 1250	Ambient temperature [°C], resolution 0.1°C

Acceleration

An internal sensor measures the acceleration.

Values	Information
-32768 to 32767	Acceleration as raw value. The conversion is to be carried out in the application: • 16 g = 32767 • -16 g = -32768

Rotation

An internal sensor measures the rotation.

Values	Information
-32768 to 32767	Rotation as raw value. The conversion is to be carried out in the application: • 2000 dps = 32767 • -2000 dps = -32768

Analog inputs

This register contains the analog input values.

Digital value	Input signal
-400 to 1250	Sensor type PT1000, Temperature measurement -40.0 to 125.0°C

Status input/output and I/O power supply

This register is used to indicate the status of the digital inputs, the digital output and the I/O power supply voltage.

Bit	Description	Value	Information
0	DigitalInput01	0 or 1	Input state - Digital input 1
1	DigitalInput02	0 or 1	Input state - Digital input 2
2 - 3	Reserved	-	
4	StateDigitalOutput01	0 or 1	Output state digital output 1
5 - 6	Reserved	-	
7	PowerSupply State of I/O power supply voltage	0	I/O power supply in the permissible range: 24 VDC -15% / +20%
		1	I/O power supply outside the permissible range

Module status

Status register for monitoring analog inputs.

Bit	Description	Value	Information
0 - 1	Channel 1	00	No error
		01	Range undershoot
		10	Range overshoot
		11	Open circuit
2 - 3	Channel 2	00	No error
		01	Range undershoot
		10	Range overshoot
		11	Open circuit
4 - 7	Reserved	-	

Switching state of the digital output

This register controls the digital output.

Bit	Description	Value	Information
0	DigitalOutput01	0	Reset output
		1	Set output
1 - 7	Reserved	0	

7.3.11.3 X20PD0011 / X20PD0012 / X20PD0016 / X20PD2113

Register	Name	Bytes	Module			
			X20PD0011 X20PD0012		X20PD0016 X20PD2113	
Input:						
0	Module status	1	Byte		Byte	
2	Supply error counter	1			Byte	
	Data bytes in DP frame		1 in	0 out	2 in	0 out

Module status

This register can be used to query the status of the built-in fuse and the power supply.

Bit	Description	Value	Information
0	Fuse	0	Fuse OK
		1	Fuse not OK
1	Voltage level (only X20PD0016 and X20PD2113)	0	Level of applied voltage OK
		1	Level of applied voltage not OK
2 - 7	Reserved	-	

Supply error counter

This register is used to count how often the voltage on the power supply module fails.

Values
0 to 255

7.3.11.4 X20PS4951

Register	Name	Bytes	Module X20PS4951	
Input:				
0	Status of the channels[1)]	1	Byte	
Data bytes in DP frame			1 in	0 out

1) Diagnostics information (overload: Channels 1 - 4) is automatically sent to the PROFIBUS DP master. Open line: Channels 1 - 4 must be evaluated via the application

Status of the channels

This register is used to show the status of the individual channels.

Bit	Name	Value	Information
0	Short circuit	0	No short circuit
		1	Short circuit on channel 1
...		...	
3	Short circuit	0	No short circuit
		1	Short circuit on channel 4
4	Open line	0	No open line
		1	Open line on channel 1
...		...	
7	Open line	0	No open line
		1	Open line on channel 4

7.3.12 Counter modules

7.3.12.1 X20CM1201

Register	Name	Bytes	Module X20CM1201	
Input:				
1	Read status	1	Byte	
3	Read parameter numbers	1	Byte	
12	Read parameter data	4	Long	
Output:				
1	Send a command	1		Byte
3	Send command parameters	1		Byte
12	Send command data	4		Long
130	Cycle time	2		1)
	Data bytes in DP frame		6 in	6 out

1) The register can be modified in the parameter dialog box for the I/O module and is transferred acyclically.

Read status

The commands and the current status can be checked in this register. Bit 7 can be used to check whether an issued command has been applied.

Bit	Description	Value	Information
0 - 1	Reserved	0	
2	Position	0	Not yet reached
		1	Reached
3	Motion	0	In motion
		1	completed
4	Counter	0	Not yet configured
		1	Configured
5	Interface	0	Not enabled
		1	Enabled
6	Command	0	No error
		1	Error occurred
7	Command toggle bit	x	Value that was read

Read parameter numbers

The parameter number returned for a display command is .

Values	Information
x	Parameter numbers

Read parameter data

The parameter data returned for a display command is .

Values	Information
x	Parameter data

Send a command

This register can be used to send commands. Bit 7 must be toggled to apply the commands. For an overview of the available commands, see the data sheet for the respective module.

Bit	Description	Value	Information
0 - 6	Command code	x	
7	Toggle bit for applying a new command	x	

Send command parameters

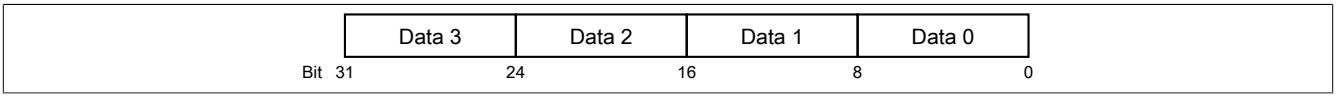
Specific parameters for the command to be sent must be entered in this register. For an overview of the required parameters, see the data sheet for the respective module.

Values	Information
x	Command parameter

Send command data

Specific parameters for the command to be sent must be entered in this register. For an overview of the available commands, see the data sheet for the respective module.

Data 0 to data 3 are sent as a single value. The following structure is used:



Values	Information
x	Command data 0 to 3

Cycle time

This register configures the module's system cycle time.

Values	Information
25 to 255	System cycle time in µs (default = 50 µs)

7.3.12.2 X20CM1941

Register	Name	Bytes	Module X20CM1941	
Input:				
0	Read angular position	4	Long	
10	**HI:** Reserved **LO:** Module status	2	Word	
Output:				
20	Offset	2		1)
22	ABR configuration	1		1)
Data bytes in DP frame			6 in	0 out

1) The register can be modified in the parameter dialog box for the I/O module and is transferred acyclically.

Read angular position

The current angle position of the resolver is . The value consists of:

- The two upper bytes, which correspond to the number of rotations counted from -32768 (0x8000xxxx) to +32767 (0x7FFFxxxx)
- The two lower bytes, which correspond to the angle position within the current rotation 1 LSB = 360° / 65536

The position value can, however, be interpreted exactly as an individual 32-bit long angle with resolution 1 / 65536 * 360°.

Values	Information
0x0000xxxx to 0xFFFFxxxx	Number of rotations (cyclic)
0xxxxx0000 to 0xxxxxFFFF	Angle position within the current rotation

Example

0x7FFF0080 corresponds to 32767 rotations, and 128 / 65536 * 360 = 0.703°.

Module status

This register shows a potential open line between the module and the encoder.

Bit	Description	Value	Information
0	Open line	0	No open line
		1	Open line
1 - 7	Reserved	-	

Offset

This register can be used to set or move the zero position for the resolver. The zero position/offset specification refers to the current resolver position.

Values
0 to 65535

ABR configuration

This register can be used to configure the resolution of the ABR emulation.

Bit	Description	Value	Information
0 - 2	Number of bits	0	8-bit = 256 increments/rotation
		1	9-bit = 512 increments/rotation
		2	10-bit = 1024 increments/rotation
		3	11-bit = 2048 increments/rotation
		4	12-bit = 4096 increments/rotation
		5 - 7	Not permitted
3 - 7	Reserved	-	

7.3.12.3 X20DC1073

Register	Name	Bytes	Module X20DC1073-C01	
Input:				
1180	Encoder position HW	2	Word	
	Encoder position LW	2	Word	
1155	**HI:** 0 **LO:** Position value counter	2	Word	
325	**HI:** 0 **LO:** Acknowledging errors	2	Word	
1212	Reference value HW	2	Word	
	Reference value LW	2	Word	
1187	**HI:** 0 **LO:**Reference value counter	2	Word	
Output:				
261	Error messages	1		Byte
Data bytes in DP frame			14 in	1 out

Support with firmware version ≥ V1.43

Encoder position

The absolute position of the encoder is defined using 32-bit resolution. The position value is stored in the PositionHW and PositionLW registers. The upper 16 bits are stored the PositionHW register, while the lower 16 bits are stored in the PositionLW register.

Values
0 to 4,294,967,295

Position value counter

This register is a cyclic counter that is incremented as soon as the module has saved a new valid position value.

Values
-128 to 127

Acknowledging errors

This register is used to acknowledge an error message that has occurred.

Bit	Name	Value	Information
0	Encoder supply error	0	No error acknowledgment
		1	Error acknowledgment
1	Reserved	-	
2	Vss error	0	No error acknowledgment
		1	Error acknowledgment
3 - 7	Reserved	-	

Reference value

The reference register prepares the value of the encoder position at the time a specific event occurred.

The 32 bit position value is placed in the two registers ReferenceHW and ReferenceLW. The upper 16 bits are in the ReferenceHW register and the lower 16 bits in the ReferenceLW register.

Values
0 to 4,294,967,295

Reference value counter

This register acts as a cyclic counter that is incremented as soon as the module has determined a new valid reference value.

Values
-128 to 127

Error messages

This register indicates which error or warning is currently active.

Bit	Name	Value	Information
0	Encoder supply	0	No error
		1	Encoder supply error
1	Reserved	-	
2	Vss error	0	No error
		1	V_{ss} error on the Sin/Cos track
3 - 7	Reserved	-	

7.3.12.4 X20DC1176 / X20DC137A

Register	Name	Bytes	Module			
			X20DC1176-C01 X20DC137A-C01*		X20DC1176-C02 X20DC137A-C02*	
Input:						
6342	ABR counter	2	Word		Word	
6310	ABR counter - Valid net time	2	Word		Word	
6358	ABR counter latch	2	Word		Word	
927	**HI:** Input status	2	Word		Word	
847	**LO:** Error messages					
Output:						
6153	**HI:** Encoder commands	2		Word		Word
811	**LO:** Acknowledge error messages					
820	Automatic error acknowledgment	4				2)
6149	Configure latch mode	1				2)
6151	Latch comparator	1				2)
Data bytes in DP frame			8 in	2 out	8 in	2 out

2) The register can be modified in the parameter dialog box for the I/O module and is transferred acyclically.

Module names with '*': Support with firmware version ≥ V1.43

ABR counter

The counter state of the incremental encoder is displayed as a 16-bit counter value.

Values
-32,768 to 32,767

ABR counter - Valid net time

The net time of the last valid counter value is the time of the last valid counter value recorded on the module. The user is able to determine the validity of the counter value by evaluating its age in the program. This means that the module and error status bits do not have to be checked additionally to determine the validity of the value.

The net time of the last valid counter value that was read is displayed as a 16-bit value.

Values	Information
-32,768 to 32,767	Net time in µs

ABR counter latch

The counter value at the time of the last latch is displayed as a 16-bit value.

Values
-32,768 to 32,767

Input status

This register displays the input status of the signal lines from the encoder and the digital inputs.

Bit	Name	Value	Information
0	Encoder channel A	0 or 1	Input state of encoder signal A
1	Encoder channel B	0 or 1	Input state of encoder signal B
2	Encoder channel R	0 or 1	Input state of encoder signal R
3	Reserved	0	
4	Digital input 1	0 or 1	Input state - Digital input 1
5	Digital input 2	0 or 1	Input state - Digital input 2
6 - 7	Reserved	0	

Error messages

This register displays the error states of the signal lines from the encoder. The error states are latched when they occur and are maintained until acknowledged. The counter and time registers are not updated if there are pending or unacknowledged errors.

Bit	Name	Value	Information
0	Encoder channel A	0	No error in encoder signal A
		1	Open line, short circuit or voltage level too low
1	Encoder channel B	0	No error in encoder signal B
		1	Open line, short circuit or voltage level too low
2	Encoder channel R	0	No error in encoder signal R
		1	Open line, short circuit or voltage level too low
3 - 7	Reserved	0	

Encoder commands

This register can be used to

1) reset the counter value. The counter is kept at zero until this command is reset.
2) enable the latch procedure. If the latch configuration is valid and matches the hardware signals, then this activation causes the counter value to be saved in the latch register.

The two different latch configurations that are possible (see section Configure latch mode) must be handled as follows:

- Single shot latch mode:
  After successful latching, indicated by the latch event counter, activation must be reset before any more latching is possible. The activation must be set again if additional latching is needed.
- Continuous latch mode:
  The latch function only has to be enabled/set as long as latching is desired. The latch event counter is incremented with each event.

Bit	Name	Value	Information
0	Reset counter	0	Do not reset
		1	Set encoder value to 0
1	Activate latch	0	Do not activate latch
		1	Latching
2 - 7	Reserved	0	

Acknowledge error messages

This register can be used to acknowledge the latched error states of the signal lines from the encoder. However, if there are still pending errors remaining, then the error status remains active. After acknowledging the errors, the bits must also be reset or else any repetition of the error would be undetected.

Bit	Name	Value	Information
0	Encoder channel A	0	No acknowledgment
		1	Acknowledgment of error status - Encoder signal A
1	Encoder channel B	0	No acknowledgment
		1	Acknowledgment of error status - Encoder signal B
2	Encoder channel R	0	No acknowledgment
		1	Acknowledgment of error status - Encoder signal R
3 - 7	Reserved	0	

Automatic error acknowledgment

This register can be used to enable an additional automatic acknowledgment of the error status using a time entry. If a valid time is set, then the acknowledgment can still be made manually, the only difference is that automatic acknowledgment will take place on the module after the defined amount of time has passed. If the error state has not yet been corrected, then the error status remains and the time is reset. Make sure that the time is set long enough for the higher-level system to reliably detect the status messages.
If the timing = 0, then acknowledgment is only possible using the cyclic acknowledgment registers.

Values	Information
0	No automatic acknowledgment
1 to 2,147,483,647	Time for automatic acknowledgment [µs]

Configure latch mode

This register is used to set the latch mode:

- Single shot latch mode configuration:
  The latch function must be enabled/set. After a successful latch procedure, the activation must be reset in order for a new latch procedure to be activated.
- Continuous latch mode:
  The latch function only has to be enabled/set as long as latching is desired.

The counter value is stored in latch register ABR counter latch.

Values	Information
0	Single shot latch procedure
1	Continuous latch procedure

Latch comparator

This register defines the signal channels and their level for triggering the latch procedure.

- This mainly configures which channels are linked to generate the latch event. All three signals from the encoder and digital input 1 can be used for the "AND" operation.
- The "active voltage level" needed for the latch procedure can now be used according to the physical signals.

Bit	Name	Value	Information
0	Defines signal level for encoder signal A	0	Low
		1	High
1	Defines signal level for encoder signal B	0	Low
		1	High
2	Defines signal level for encoder signal R	0	Low
		1	High
3	Defines signal level for digital input 1	0	Low
		1	High
4	Use encoder signal A to trigger latch procedure	0	Disabled
		1	Latch function linked to encoder signal A
5	Use encoder signal B to trigger latch procedure	0	Disabled
		1	Latch function linked to encoder signal B
6	Use encoder signal R to trigger latch procedure	0	Disabled
		1	Latch function linked to encoder signal R
7	Use digital input 1 to trigger latch procedure	0	Disabled
		1	Latch function linked to digital input 1

7.3.12.5 X20DC1178

Register	Name	Bytes	Module X20DC1178-C01	
Input:				
2100	SSI position	4	Long	
2086	Counter - Valid net time	2	Word	
927	**HI:** Digital inputs	2	Word	
259	**LO:** Error messages			
Output:				
323	Acknowledge error messages	1		Byte
Data bytes in DP frame			8 in	1 out

SSI position

The counter state of the incremental encoder is displayed as a 32-bit counter value.

Values
0 to 4,294,967,295

Counter - Valid net time

The net time of the last valid counter value is the time of the last valid counter value recorded on the module. The user is able to determine the validity of the counter value by evaluating its age in the program. This means that the module and error status bits do not have to be checked additionally to determine the validity of the value.

The net time of the last valid counter value that was read is displayed as a 16-bit value.

Values	Information
-32,768 to 32,767	Net time in µs

Digital inputs

This register displays the input states for the digital inputs.

Bit	Name	Value	Information
0 - 3	Reserved	0	
4	Input 1	0 or 1	Input state - Digital input 1
5	Input 2	0 or 1	Input state - Digital input 2
6 - 7	Reserved	0	

Error messages

This register displays the error states that occurred while determining the position. The error states are latched when they occur and are maintained until acknowledged.

A cycle time error is triggered if:

- Transfer is still active: This means that the defined cycle time is shorter than the time resulting from the sum of the data bits and stop bits and the clock rate.
- The monoflop level does not match the defined start level
- There is an error pending on the signal line (open line, short circuit).

A data error is triggered if:

- The parity bit does not match.
- An error occurs on the signal line (open line, short circuit) during transfer.

Bit	Name	Value	Information
0	Cycle time violation	0	No error
		1	Error status - Cycle time violation
1	Data error	0	No error
		1	Error status - Data error
2 - 7	Reserved	0	

Acknowledge error messages

This register can be used to acknowledge the latched data error states from the encoder. However, if there are still pending errors remaining, then the error status remains active. After acknowledging the errors, the bits must also be reset or else any repetition of the error would be undetected.

Bit	Name	Value	Information
0	Cycle time violation	0	No acknowledgment
		1	Confirmation of error status - Cycle time violation
1	Data error	0	No acknowledgment
		1	Confirmation of error status - Data error
2 - 7	Reserved	0	

7.3.12.6 X20DC1x96

Register	Name	Bytes	Module			
			X20DC1196-C01 X20DC1396-C01		X20DC1196-C02 X20DC1396-C02	
Input:						
2080	ABR counter 1	2	Word		Word	
40 264	**HI:** Status of encoder supply **LO:** Encoder inputs and digital inputs	2	Word		Word	
2118	**HI:** 0 **LO:** Status of the homing procedure 1	2	Word		Word	
Output:						
2116	Referencing mode 1	1		Byte		Byte
512	Referencing mode - Edge selection 1	1				1)
520	Reference enable 1	1				1)
522	Reference enable - Voltage level 1	1				1)
2064	Homing position 1	2				1)
Data bytes in DP frame			6 in	1 out	6 in	1 out

1) The register can be modified in the parameter dialog box for the I/O module and is transferred acyclically.

ABR counter

This register indicates the encoder values as 16-bit counter values.

Values
-32,768 to 32,767

Status of encoder supply

This register indicates the status of the integrated encoder supply. A faulty encoder power supply is displayed as a warning.

Bit	Name	Value	Information
0	Supply voltage	0	24 VDC encoder power supply OK
		1	24 VDC encoder power supply faulty
1 - 7	Reserved	-	

Encoder inputs and digital inputs

This register displays the input status of the encoders and the digital inputs.

Bit	Name	Value	Information
0	Encoder A	0 or 1	Input state
1	Encoder B	0 or 1	Input state
2	Encoder A + B	0 or 1	Input state of reference pulse
4	Digital input 1	0 or 1	Input state - Digital input 1
5	Digital input 2 (only X20DC1396 module)	0 or 1	Input state - Digital input 2
4 or 5 - 7	Reserved	0	

Status of the homing procedure

This register contains information regarding whether the referencing process is off, active or complete.

Bit	Name	Value	Information
0	Reference pulse without homing[1)]	0	No reference impulse without homing has occurred yet
		1	At least a reference impulse without homing has occurred
1	State change	0 or 1	Changes with each reference pulse without homing
2	Reference pulse with homing[1)]	0	No homing has occurred yet
		1	At least one homing procedure has occurred
3	State change	0 or 1	Changes with each homing procedure that has taken place
4	Reference pulse	0	The last reference pulse didn't bring about a homing procedure
		1	The last reference pulse brought about a homing procedure
5 - 7	Counter	x	Free-running counter, increased with each reference pulse

1) Always 1 after the first reference pulse that has occurred

Examples of possible values:

Binary	Hex	Function
0x00000000	0x00	Referencing OFF or homing procedure already active
0x00111100	0x3CE	First homing procedure complete Reference value applied in the ABR counter register
0xxxx11100	0xxB	Bits 5 to 7 are changed with each reference pulse
0xxxx1x100	0xxx	Continuously changing the bits with the "Continuous referencing" setting. The reference value is applied to the ABR counter register on each reference pulse.

It is important to know how the optional reference enable is configured. See the section Homing with reference enable input.

Referencing mode

This register determines the referencing mode.

Bit	Name	Value	Information
0 - 1		00	Referencing OFF
		01	Single shot referencing
		11	Continuous referencing
2 - 5		0	Bits permanently set = 0
6 - 7		00	Referencing OFF
		11	Bits permanently set = 1

This results in the following values:

Binary	Hex	Function
00000000	0x00	Referencing OFF
11000001	0xC1	Single shot referencing For a new start after the completed homing procedure: • Write value 0x00 • Wait until bit 0 to bit 3 of the Status of the homing procedure register takes on the value 0. Counter bits 4 to 7 are not erased • Switch homing procedure on again
11000011	0xC3	Continuous referencing Referencing occurs at every reference pulse.

It is important to know how the optional reference enable is configured. See the section Homing with reference enable input.

Referencing mode - Edge selection

This register contains the value for the ABR encoder.

Values	Filter
0x1012	Configuration value for rising edge
0x1002	Configuration value for falling edge

Homing with reference enable input

Regardless of the referencing mode, it is possible using the next two registers to prevent the home position from being applied when the corresponding reference input voltage level occurs (see Encoder inputs and digital inputs: Bit 4). The desired setting can be configured by a one-off acyclic write.

Reference enable

This register can be used to define whether the reference enable is activated.

Values	Filter
0x00	Reference enable input OFF (default)
0x08	Only X20DC1396: Reference enable input
0x10	Only X20DC1196: Reference enable input 1 enabled
0x20	Only X20DC1196: Reference enable input 2 enabled
0x30	Only X20DC1196: Reference enable input 1 and 2 enabled

Reference enable - Voltage level

The voltage level of the digital inputs to activate reference enable is configured with this register.

Values	Filter
0x00	Reference enable is active at 0 VDC
0x08	OnlyX20DC1396: Reference enable is active at 24 VDC
0x10	Only X20DC1196: Reference enable for digital input 1 is active at 24 VDC
0x20	Only X20DC1196: Reference enable for digital input 2 is active at 24 VDC
0x30	Only X20DC1196: Reference enable for both digital inputs is active at 24 VDC

Homing position

It is possible to specify two home positions with these registers through a one-off acyclic write, for example (default = 0). The configured values are applied to the counter values after a completed homing procedure.

Values
-32,768 to 32,767

7.3.12.7 X20DCxx98

Register	Name	Bytes	Module			
			X20DC1198-C01 X20DC1398-C01		X20DC2398-C01	
Input:						
7184	SSI position 1	4	Long		Long	
40	**HI:** Status of encoder supply	2	Word		Word	
264	**LO:** Digital inputs					
7440	SSI position 2	4			Long	
Output:						
0	Reserved	1		Byte		Byte
Data bytes in DP frame			6 in	1 out	10 in	1 out

SSI position

The two SSI encoder values are displayed as 32-bit position values. The SSI position values are generated synchronously with the X2X cycle.

Values
0 to 4,294,967,729

Status of encoder supply

This register indicates the status of the integrated encoder supply. A faulty encoder power supply is displayed as a warning.

Bit	Name	Value	Information
0	Supply voltage	0	24 VDC encoder power supply OK
		1	24 VDC encoder power supply faulty
1 - 7	Reserved	-	

Digital inputs

This register is used to indicate the input state of digital inputs 1 to 2.

Bit	Name	Value	Information
3	DigitalInput01	0 or 1	Input state - Digital input 1
7	DigitalInput02	0 or 1	Input state - Digital input 2

7.3.12.8 X20DC2190

Register	Name	Bytes	Module			
			X20DC2190		X20DC2190-C5	
Input:						
0	Position 1	4	Long		Long	
4	Position 2	4	Long		Long	
8	Position 3	4	Long		Long	
12	Position 4	4	Long		Long	
16	Speed 1	2	Word		Word	
18	Speed 2	2	Word		Word	
20	Speed 3	2	Word		Word	
22	Speed 0	2	Word		Word	
38	**HI:** Status of the transducer rods **LO:** Error status 1	2	Word		Word	
40	**HI:** 0 **LO:** Error status 2	2	Word		Word	
42	**HI:** 0 **LO:** Error status 3	2	Word		Word	
44	**HI:** 0 **LO:** Error status 4	2	Word		Word	
Output:						
30	Configuration of the measurement rate 01	4		Long		Long
34	Configuration of the measurement rate 02	4		Long		Long
68	**HI:** 0 **LO:** Set the zero position	2		Word		Word
2200	Module configuration			1)		
2100	Channel configuration			1)		
2000	Rod length 1			1)		
2004	Rod length 2			1)		
2008	Offset position 1			1)		
2012	Offset position 2			1)		
2024	Minimum magnet position 1			1)		
2028	Minimum magnet position 2			1)		
2040	Maximum magnet position 1			1)		
2044	Maximum magnet position 2			1)		
2056	Magnet speed 1			1)		
2060	Magnet speed 2			1)		
2016	Offset position 3			1)		
2020	Offset position 4			1)		
2032	Minimum magnet position 3			1)		
2036	Minimum magnet position 4			1)		
2048	Maximum magnet position 3			1)		
2052	Maximum magnet position 4			1)		
2064	Magnet speed 3			1)		
2068	Magnet speed 4			1)		
2201	Dead time 1			1)		
2202	Dead time 2			1)		
Data Bytes in DP Frame			32 in	10 out	32 in	10 out

1) The register is transferred acyclically.

Position

These registers contain the position of the individual magnets on the transducer rods.

Values	Information
-2,147,483,648 to 2,147,483,647	Resolution 1 µm

Speed

These registers contain the speed of the individual magnets on the transducer rods. A resolution of 0.1 mm/s is achieved by calculating the speed from 2 position values within a 100 ms interval.

Values	Information
-32,768 to 32,767	Resolution 0.1 mm/s

Status of the transducer rods

This register displays the status information for the transducer rods.

Bit	Name	Value	Information
0	Supply voltage too low	0	Supply voltage OK
		1	Supply voltage too low
1	Supply voltage too high	0	Supply voltage OK
		1	Supply voltage too high
2	Transducer Rod 1	0	OK
		1	Deactivated or not initialized
3	Transducer Rod 2	0	OK
		1	Deactivated or not initialized
4	Transducer Rod 1	0	Protocol error (invalid data)
		1	Protocol OK (valid data)
5	Transducer Rod 2	0	Protocol error (invalid data)
		1	Protocol OK (valid data)
6 - 7	Reserved	-	

Comment concerning bits 4 + 5

If this bit is set to "1", configuration data was successfully read from the measurement rod using DPI/IP or EP protocol. This data can now be read into the application using asynchronous access.

Error status

These registers are used to indicate the error status for individual channels.

Bit	Name	Value	Information
0 - 3	Counter for plausibility errors (cyclic)	x	
4 - 7	Counter for mis-measurements (cyclic)	x	

Possible reasons for plausibility errors:

- Configured maximum or minimum path of a magnet was exceeded
- Configured maximum speed was exceeded

Possible reasons for faulty measurements:

- Configured rod length was exceeded
- Rod failure
- Missing measurement magnet

Configuration of the measurement rate

The module does not perform any measurements on the respective rod while these registers have the value 0. Also disabled:

- Automatic check to determine whether a rod is connected
- Parameter upload via DPI/IP or EP protocol

If a value >0 but <1000cm/s is specified here, the module freezes all measurements and error counters of the corresponding rod, regardless of whether plausibility mode is enabled or not. Based on the default ultrasonic speed of 280,000 cm/s, however, periodic measurement start pulses continue to be generated according to the formula in section Channel configuration. In this case the rod check (inserted/not inserted and parameter upload) continues to be active.

As soon as a valid value (≥1000) is specified, the module recalculates the measurement rate and begins the position/speed measurement.

Values	Information
0 to 4,294,967,296	Resolution 1 cm/s

Set the zero position

This register makes it easier to more quickly determine new offsets (= zero positions) for the individual magnets. This approach is an alternative or additional method to determining an offset via configuration registers (see Offset position).

If the respective bit changes from 0 to 1 in this register then the current mechanical position of the respective magnet becomes the calculated zero position.
From that moment, the current mechanical position will be subtracted from all future measured positions. This is essentially a type of referencing. The maximum and minimum magnet paths are now based on the new zero position.
This process can be repeated at any time by setting the bit again.

Information:

An offset position determined in this manner cannot be read out.

Bit	Name	Value	Information
0	Magnet 1	0	No effect
		1	Apply offset magnet 1
...		...	
3	Magnet 4	0	No effect
		1	Apply offset magnet 4
4 - 7	Reserved	-	

Module configuration

This register configures the module.

Bit	Name	Value	Information
0	Plausibility mode	0	The plausibility error counter is incremented with each implausible measurement and the last plausible measurement value is "frozen" (default)
		1	The plausibility error counter is incremented with each implausible measurement and the implausible measurement value is forwarded to the controller
1	Reserved	-	
2 - 3	Tolerance for monitoring the supply voltage	00	25%
		01	20%
		10	15%
		11	10%
4 - 7	Magnet number	0000	4 magnets on channel 1, channel 2 not available
		0001	3 magnets on channel 1, 1 magnet on channel 2
		0010	2 magnets on channel 1, 2 magnets on channel 2
		0011	1 magnet on channel 1, 0 magnets on channel 2
		0100	2 magnets on channel 1, 0 magnets on channel 2
		0101	3 magnets on channel 1, 0 magnets on channel 2
		0110	2 magnets on channel 1, 1 magnet on channel 2
		0111	1 magnet on channel 1, 1 magnet on channel 2
		1xxx	Reserved

Channel configuration

This register can be used to configure the individual channels.

Bit	Description	Value	Information
0 - 2	Transducer Rod 1	000	User parameter
		001	DPI/IP (Balluf)
		010	EP Start/Stop (MTS)
		011	Reserved
		1xx	Reserved
3 - 4	Rod 1: Start/Stop IF type	00	Start/Stop Signal: Rising edge - rising edge
		01	Start/Stop Signal: Falling edge - falling edge
		10	Start/Stop Signal: Rising edge - falling edge (gate time)
		11	Only Stop Signal: Start when signal is triggered (initialization pulses)
5	Rod 1: Recovery time factor, minimum time between two measurements	0	3 x USW runtime for rod (default)
		1	2 x USW runtime for rod
6 - 7	Reserved	-	
8 - 10	Transducer Rod 2	000	User parameter
		001	DPI/IP (Balluf)
		010	EP Start/Stop (MTS)
		011	Reserved
		1xx	Reserved
11 - 12	Rod 2: Start/Stop IF type	00	Start/Stop Signal: Rising edge - rising edge
		01	Start/Stop Signal: Falling edge - falling edge
		10	Start/Stop Signal: Rising edge - falling edge (gate time)
		11	Only Stop Signal: Start when signal is triggered (initialization pulses)
13	Rod 2: Recovery time factor, minimum time between two measurements	0	3 x USW runtime for rod (default)
		1	2 x USW runtime for rod
14 - 15	Reserved	-	

USW transducer rods require a certain recovery time between 2 measurements to allow the ultrasonic wave to fade. Otherwise there is a risk of interfering with the next measurement (especially when the rod has more than 1 magnet).

Depending on the setting, the module waits at least 2 or 3 times the runtime of the ultrasonic wave for the measurement rod (default = 3x). In the standard function module, the next measurement is then triggered synchronously with the next X2XLink cycle.

The runtime measurement is based on the settings for the rod length (plus a safety margin of 100mm) and the ultrasonic speed:

- USW runtime = (rod length + 100mm) / ultrasonic speed.

For their rods, BALLUFF recommends a recovery time equal to 3 times the maximum runtime of the ultrasonic wave for the measurement rod. This is the default setting for the module.

The setting can be switched to 2 times the runtime if the measurement rate is otherwise too slow. This may only be done after consulting the manufacturer of the transducer rods!

Rod length

These registers are used to configure the length of the respective rod.

Values	Information
0 to 4,294,967,296	Resolution 1 mm

Offset position

These registers are used to assign the respective magnet an offset position (= zero position) on the transducer. The maximum and minimum magnet paths refer to these specified offsets. If the offset is changed using the Set the zero position register, this becomes the new zero position. This does not affect the contents of the offset register.

Values	Information
-2,147,483,648 to 2,147,483,647	Resolution 1 µm

Minimum magnet position

These registers are used to assign the minimum plausible magnet position based on the applicable offset.

Values	Information
-2,147,483,648 to 2,147,483,647	Resolution 1 µm

Maximum magnet position

These registers are used to assign the maximum plausible magnet position based on the applicable offset.

Values	Information
-2,147,483,648 to 2,147,483,647	Resolution 1 µm

Magnet speed

These registers are used to assign the max. plausible magnet speed.

Values	Information
0 to 4,294,967,296	Resolution 0.1 mm/s

Dead time

These registers are used to configure the dead time of the respective rod.

To prevent the multiple pulses that occur with some encoders from affecting the measurement, all pulses received within a configurable timespan from the beginning of the measurement are not evaluated. The range for the dead time lies between 0 and 255 µs. The following figure illustrates the effects of defining a dead time:

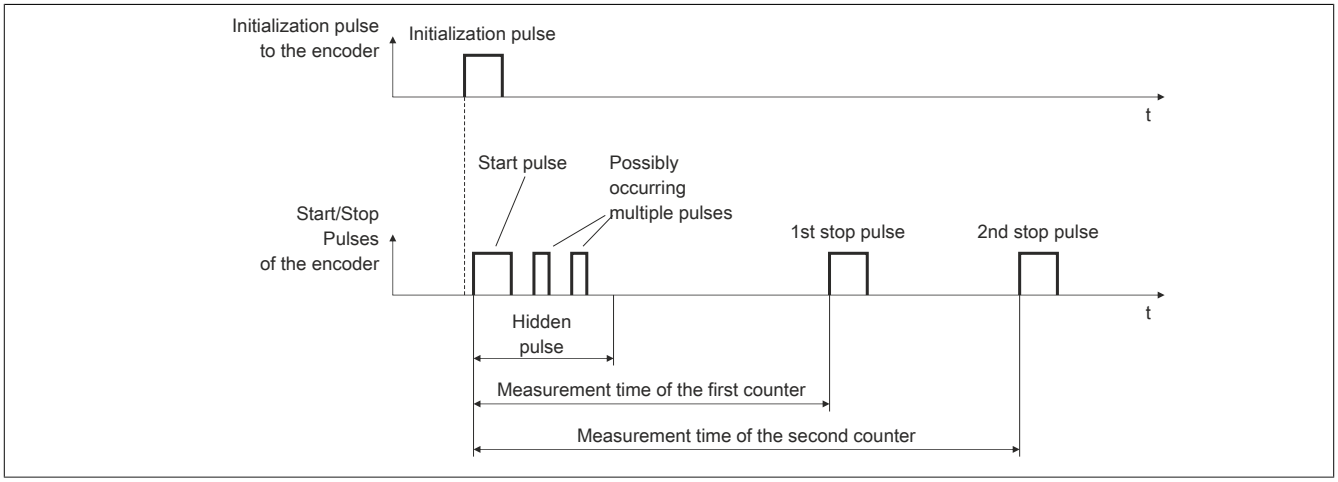


Figure 4: Pulse Ignored after Start Pulse

Values	Information
0 to 255	Resolution 1 µs (default: 0 µs)

7.3.12.9 X20DC2395

Register	Name	Bytes	Module X20DC2395-C01	
Input:				
2080	Event counter Channel 1	2	Word	
2336	Event counter Channel 3	2	Word	
40	**HI: 0** **LO:** Status of encoder supply	2	Word	
Output:				
6146	PWM output Channel 2	2		Word
6162	PWM output Channel 4	2		Word
2056	Configuration of the counter calculation Channel 1	1		1)
2312	Counter value calculation Channel 3	1		1)
6144	PWM cycle time Channel 2	2		1)
6160	PWM cycle time Channel 4	2		1)
Data bytes in DP frame			6 in	4 out

1) The register can be modified in the parameter dialog box for the I/O module and is transferred acyclically.

Event counter

These 4 registers show the results of the Counter value calculation for the respective register. Depending on the function, this corresponds to either the encoder position or the counter value.

Value	Information
-32,768 to 32,767	Encoder position or counter value

1) Only in function model 1

Status of encoder supply

This register indicates the status of the integrated encoder supply. A faulty encoder power supply is displayed as a warning.

Bit	Name	Value	Information
0	Supply voltage	0	24 VDC encoder power supply OK
		1	24 VDC encoder power supply faulty
1 - 7	Reserved	-	

PWM output

In this register, a configuration is made for the percentage of the PWM cycle (in 1/10 % steps) that the PWM output is logical 1, i.e. ON.

Value	Information
0 to 1000	PWM output always off
2 to 999	Turn on time in 1/10% steps
1000	PWM output always on

Counter value calculation

There are 3 steps for calculating the state of any counter function

1. The counter value is based on the 2 absolute value counters "abs1" and "abs2". They are only used internally in the module and cannot be read.

	Mode
	Edge counters
abs1	Edges of counter channel 1
abs2	Edges of counter channel 2

2. From the absolute value registers "abs1" and "abs2", 2 more counters are formed: "counter 1" and "counter 2". These are only used internally in the module and cannot be read.

3. The counter registers contain the sum of the two internal counters "counter 1" and "counter 2". The Configuration of the counter calculation register allows you to define a sign for each "counter" register and define whether or not it should be used.

Counter register = counter1 + counter2

Configuration of the counter calculation

The calculation of internal registers "counter1" and "counter2" can be configured in these registers. For information about using these internal registers, see Counter value calculation.

Bit	Description	Value	Information
0	counter 1 - use	0	0 is added instead of "counter 1"
		1	"counter 1" is used for addition
1	counter 1 - sign	0	The sign of the "counter 1" register is not changed for addition
		1	The sign of the "counter 1" register is reversed for addition
2	counter 2 - use	0	0 is added instead of "counter 2"
		1	"counter 2" is used for addition
3	counter 2 - sign	0	The sign of the "counter 2" register is not changed for addition
		1	The sign of the "counter 2" register is reversed for addition
4 - 7	Reserved	-	

Examples of calculation configurations

0b00000001	= 0x01	Only the "counter1 - use" bit is set, entering the contents of the "counter" (edge of counter event channel 1) directly in the counter register.
0b00000011	= 0x03	"counter 1 - use" and "counter1 - sign" bits are set. The sign is changed so that the counter register counts in the negative direction.
0b00001101	= 0x0d	Edges on counter input channel 1 increase the value in the counter register. Edges on counter input channel 2 decrease the value in the counter register. This value is the best setting for the modes "AB encoder" and "Up/down counter".

PWM cycle time

The length of the PWM cycle is configured using this register. The base is a 48 MHz clock, which can be changed (divided) using the setting in this register. One PWM cycle consists of 1,000 of the resulting clocks after they have been divided. The period duration of the PWM cycle is calculated as follows:

$$PWM_cycle = 1000 \frac{prescale}{48000000} [s]$$

Value	Information
2 to 65,535	Prescaler for PWM cycle

7.3.12.10 X20DC2396

Register	Name	Bytes	Module			
			X20DC2396-C01		X20DC2396-C02	
Input:						
2080	ABR counter Channel 1	2	Word		Word	
40	**HI:** Status of encoder supply	2	Word		Word	
264	**LO:** Encoder inputs and digital inputs 1 - 2					
2592	ABR counter Channel 2	2	Word		Word	
2630	**HI:** Status of the homing procedure 2	2	Word		Word	
2118	**LO:**Status of the homing procedure 1					
Output:						
2116	Homing mode 1	1		Byte		Byte
2628	Homing mode 2	1		Byte		Byte
512	Referencing mode - Edge selection Channel 1	1				1)
520	Reference enable Channel 1	1				1)
522	Reference enable - Voltage level Channel 1	1				1)
2064	Homing position Channel 1	2				1)
544	Referencing mode - Edge selection Channel 2	1				1)
552	Reference enable Channel 2	1				1)
554	Reference enable - Voltage level Channel 2	1				1)
2576	Homing position Channel 2	2				1)
Data bytes in DP frame			8 in	2 out	8 in	2 out

1) The register is transferred acyclically.

ABR counter

The encoder values are displayed in this register.

Values
-32,768 to 32,767

Status of encoder supply

This register indicates the status of the integrated encoder supply. A faulty encoder power supply is displayed as a warning.

Bit	Name	Value	Information
0	Supply voltage	0	24 VDC encoder power supply OK
		1	24 VDC encoder power supply faulty
1 - 7	Reserved	-	

Encoder inputs and digital inputs

This register displays the input status of the encoders and the digital inputs.

Bit	Name	Value	Information
0	Encoder 1	0 or 1	Input state - Signal A
1		0 or 1	Input state - Signal B
2		0 or 1	Input state of reference pulse
3	Digital input 1	0 or 1	Input state - Digital input 1
4	Encoder 2	0 or 1	Input state - Signal A
5		0 or 1	Input state - Signal B
6		0 or 1	Input state of reference pulse
7	Digital input 2	0 or 1	Input state - Digital input 2

Status of the homing procedure

This register contains information regarding whether the referencing process is off, active or complete.

Bit	Name	Value	Information
0	Reference pulse without homing[1)]	0	No reference impulse without homing has occurred yet
		1	At least a reference impulse without homing has occurred
1	State change	0 or 1	Changes with each reference pulse without homing
2	Reference pulse with homing[1)]	0	No homing has occurred yet
		1	At least one homing procedure has occurred
3	State change	0 or 1	Changes with each homing procedure that has taken place
4	Reference pulse	0	The last reference pulse didn't bring about a homing procedure
		1	The last reference pulse brought about a homing procedure
5 - 7	Counter	x	Free-running counter, increased with each reference pulse

1) Always 1 after the first reference pulse that has occurred

Examples of possible values:

Binary	Hex	Function
0x00000000	0x00	Referencing OFF or homing procedure already active
0x00111100	0x3CE	First homing procedure complete Reference value applied in the ABR counter register
0xxxx11100	0xxB	Bits 5 to 7 are changed with each reference pulse
0xxxx1x100	0xxx	Continuously changing the bits with setting "Continuous referencing". The reference value is applied to the ABR counter register on each reference pulse.

It is important to know how the optional reference enable is configured. See section Homing with reference enable input.

Homing mode

This register determines the referencing mode.

Bit	Name	Value	Information
0 - 1		00	Referencing OFF
		01	Single shot referencing
		11	Continuous referencing
2 - 5		0	Bits permanently set = 0
6 - 7		00	Referencing OFF
		11	Bits permanently set = 1

This results in the following values:

Binary	Hex	Function
00000000	0x00	Referencing OFF
11000001	0xC1	Single shot referencing For a new start after the completed homing procedure: • Write value 0x00 • Wait until bit 0 to bit 3 of the StatusInput01 register takes on the value 0. Counter bits 4 to 7 are not erased • Switch homing procedure on again
11000011	0xC3	Continuous referencing Referencing occurs at every reference pulse.

It is important to know how the optional reference enable is configured. See section Homing with reference enable input.

Referencing mode - Edge selection

This register contains the value for the ABR encoder. Configuration on rising or falling edge of the reference pulse is necessary for continual referencing (cyclic operation), in order to complete the referencing procedure.

Values	Information
0x1012	Configuration value for rising edge
0x1002	Configuration value for falling edge

Homing with reference enable input

Regardless of the referencing mode, it is possible using the next two registers to prevent the home position from being applied when the corresponding reference input voltage level occurs (see Encoder inputs and digital inputs: bit 4). The desired setting can be configured by a one-off acyclic write.

Reference enable

This register can be used to define whether the reference enable is activated.

Values	Information
0x00	Reference enable input OFF (default)
0x08	Reference enable input activated

Reference enable - Voltage level

The voltage level of the digital input 1 to activate reference enable is configured with this register.

Values	Information
0x00	Reference enable is active at 0 VDC
0x08	Reference enable is active at 24 VDC

Homing position

It is possible to specify two home positions for each encoder with these registers through a one-off acyclic write, for example (default = 0). The configured values are applied to the counter values after a completed homing procedure.

Values
-32,768 to 32,767
-2,147,483,648 to 2,147,483,647

7.3.12.11 X20DC4395

Register	Name	Bytes	Module X20DC4395-C01	
Input:				
7184	SSI position Channel 1	4	Long	
2336	Event counter Channel 3	2	Word	
2592	ABR counter Channel 5 - 7	2	Word	
2630	**HI:** ABR status of the homing procedure	2	Word	
40	**LO:** Status of encoder supply			
Output:				
6162	PWM output Channel 4	2		Word
6194	PWM output Channel 8	2		Word
2628	**HI:** 0 **LO:** ABR referencing mode	2		Word
7172	SSI configuration	4[1)]		
6160	PWM cycle time Channel 4	2		[2)]
6192	PWM cycle time Channel 8	2		[2)]
2312	Configuration of the counter calculation	1		[2)]
2576	ABR homing position	2		[2)]
544	ABR reference switch edge	1		[2)]
Data bytes in DP frame			10 in	6 out

1) This register is configured as individual bytes by the PROFIBUS DP master in the following order: SSI baud rate, SSI value, SSI data format, number of SSI bits.
2) The register is transferred acyclically.

SSI position

The last transferred SSI position can be read out from this register. The SSI encoder value is displayed as a 32-bit position value. This position value is generated synchronously with the X2X cycle.

Value	Information
0 to 4,294,967,295	Last SSI position transferred

Event counter

In these registers, the result of Counter value calculation is displayed for the respective register. Depending on the function, this corresponds to either the encoder position or the counter value.

Value	Information
-32,768 to 32,767	Encoder position or counter value

ABR counter

In these registers, the counter value of the encoder is displayed for the respective register on channels 5 to 7 on the module connections per Counter value calculation.

Value	Information
-32,768 to 32,767	Counter value

ABR status of the homing procedure

This register contains the homing state of the ABR encoder.

Bit	Description	Value	Information
0 - 1	Reserved	0	
2	Bit is always 1 after the first reference pulse.	0	No reference pulses have occurred since the start of referencing.
		1	The first reference pulse has occurred.
3	State change when referencing is complete	0 or 1	State change when referencing is complete
4	Bit is always 1 after the first reference pulse.	0	No reference pulses have occurred since the start of referencing.
		1	The first reference pulse has occurred.
5 - 7	Continuous counter	xxx	Increased with each reference pulse

Examples of possible values

0b00000000	= 0x00	Referencing OFF or homing procedure already active
0b00111100	= 0x3C	First reference complete, reference value applied in the ABR counter register.
0bxxx11100	= 0xxB	Bits 5 to 7 are changed with each reference pulse
0bxxx1x100	= 0xxx	Bits changed continuously with the setting continuous referencing. With every reference pulse, the reference value is applied to the ABR counter register.

Status of encoder supply

This register indicates the status of the integrated encoder supply. A faulty encoder power supply is displayed as a warning.

Bit	Name	Value	Information
0	Supply voltage	0	24 VDC encoder power supply OK
		1	24 VDC encoder power supply faulty
1 - 7	Reserved	-	

PWM output

In this register, a configuration is made for the percentage of the PWM cycle (in 1/10 % steps) that the PWM output is logical 1, i.e. ON.

Value	Information
0	PWM output always off
2 to 999	Turn on time in 1/10% steps
1000	PWM output always on

ABR referencing mode

The bits in this register are used to configure the reaction to the configured reference pulse.

Bit	Description	Value	Information
0 - 1	Sets the referencing mode	00	Referencing OFF
		01	Single shot referencing
		10	Reserved
		11	Continuous referencing
2 - 5	Reserved	-	
6 - 7	Reserved	11	Must always be 11!

This results in the following values:

0b00000000	= 0x00	Referencing OFF
0b11000001	= 0xC1	Single-shot referencing →When starting over after the referencing process is complete, the value 0x00 must be written to start again. Wait until the ABR status of the homing procedure register also takes on the value 0x00. Only then is value 0xC1 permitted to be written again.
0b11000011	= 0xC3	Continuous referencing →Referencing takes place automatically with every reference pulse

SSI configuration

This configuration register is used to set the coding, the clock rate, the number of bits and the monostable multivibrator settings.
Default = 0.

Bit	Name	Value	Information
0 - 5	SSI value valid bits	x	
6 - 7	Clock rate	11	125 kHz
8 - 13	SSI number of bits	x	Number of bits including leading zeros
14	Reserved	0	
15	Keying	0	Binary coding
		1	Gray coding
16 - 17	Monostable multivibrator check	00	Check OFF, no additional clock bit
		01	Check set to High level
		10	Check set to Low level
		11	Level is clocked but ignored
18 - 31	Reserved	0	

PWM cycle time

The length of the PWM cycle is configured using this register. The base is a 48 MHz clock, which can be changed (divided) using the setting in this register. One PWM cycle consists of 1,000 of the resulting clocks after they have been divided. The period duration of the PWM cycle is calculated as follows:

$$PWM_cycle = 1000 \frac{prescale}{48000000} [s]$$

Value	Information
2 to 65,535	Prescaler for PWM cycle

Counter value calculation

There are 3 steps for calculating the state of any counter function

1. The counter value is based on the 2 absolute value counters "abs1" and "abs2". These are only used internally in the module and cannot be read.

	Mode	
	Edge counters	AB encoders
abs1	Edges of counter channel 1	Increments in positive direction
abs2	Edges of counter channel 2	Increments in negative direction

2. From the absolute value registers "abs1" and "abs2", 2 more counters are formed: "counter 1" and "counter 2". They are only used internally in the module and cannot be read. The following values are used for the calculation:

- Absolute value registers "abs1" and "abs2"
- SW_reference_counter 1 and 2: This reference value can be defined by the ABR homing position register to allow referencing <> 0.

counter1 = abs1 + SW_reference_counter1
counter2 = abs2 + SW_reference_counter2

3. The counter registers contain the sum of the two internal counters "counter 1" and "counter 2". The Configuration of the counter calculation register allows you to define a sign for each "counter" register and define whether or not it should be used.

Counter register = counter1 + counter2

Configuration of the counter calculation

The calculation of internal registers "counter1" and "counter2" can be configured in these registers. For information about using these internal registers, see Counter value calculation.

Bit	Description	Value	Information
0	counter 1 - use	0	0 is added instead of "counter 1"
		1	"counter 1" is used for addition
1	counter 1 - sign	0	The sign of the "counter 1" register is not changed for addition
		1	The sign of the "counter 1" register is reversed for addition
2	counter 2 - use	0	0 is added instead of "counter 2"
		1	"counter 2" is used for addition
3	counter 2 - sign	0	The sign of the "counter 2" register is not changed for addition
		1	The sign of the "counter 2" register is reversed for addition
4 - 7	Reserved	-	

Examples of calculation configurations

0b00000001	= 0x01	Only the "counter1 - use" bit is set, entering the contents of the "counter" (edge of counter event channel 1) directly in the counter register.
0b00000011	= 0x03	"counter 1 - use" and "counter1 - sign" bits are set. The sign is changed so that the counter register counts in the negative direction.
0b00001101	= 0x0d	Edges on counter input channel 1 increase the value in the counter register. Edges on counter input channel 2 decrease the value in the counter register. This value is the best setting for the modes "AB encoder" and "Up/down counter".

ABR homing position

These registers can be used to define an offset value for referencing. This value is copied to internal register SW_reference_counter (see Counter value calculation) of the respective counter register. (High byte = counter value homing position / 256 (without remainder), Low byte = remainder * 256)

Values
-32,768 to 32,767

ABR reference switch edge

This register configures whether a rising or falling edge is used to trigger referencing.

Value	Information
4102	Falling edge
4118	Rising edge
4134	Falling or rising edge

7.4 X67 I/O system

7.4.1 Digital input modules

7.4.1.1 X67DI137x

Register	Name	Bytes	Module			
			X67DI1371-C01 X67DI1372		X67DI1371.L08-C01 X67DI1371.L12-C01	
Input:						
0	Digital inputs 1 - 8	1	Byte		Byte	
1	Digital inputs 9 - 16	1			Byte	
Data bytes in DP frame			1 in	0 out	2 in	0 out

Digital inputs 1 - 8

This register is used to indicate the input state of digital inputs 1 to 8. As a result, the input with the lowest channel number is located in the LSB; the bits of the inputs that are not present are 0.

Bit	Name	Value	Information
0	Channel 1	0 or 1	Input state - Digital input 1
...		...	
7	Channel 8	0 or 1	Input state - Digital input 8

Digital inputs 9 - 16

This register is used to indicate the input state of digital inputs 9 to 16. As a result, the input with the lowest channel number is located in the LSB; the bits of the inputs that are not present are 0.

Bit	Name	Value	Information
0	Channel 9	0 or 1	Input state - Digital input 9
...		...	
3	Channel 16	0 or 1	Input state - Digital input 16

7.4.2 Digital output modules

7.4.2.1 X67DO1332

Register	Name	Bytes	Module			
			X67DO1332-C01		X67DO1332-C02	
Input:						
2	Status of the outputs[1)]	1			Byte	
Output:						
30	Digital outputs 1 - 8	1		Byte		Byte
Data bytes in DP frame			0 in	1 out	1 in	1 out

1) Diagnostics information is automatically sent to the PROFIBUS DP master.

Status of the outputs

This register is used to indicate the status of the digital outputs.

Bit	Name	Value	Information
0	Channel 1	0	No error
		1	Short circuit or overload
...		...	
7	Channel 8	0	No error
		1	Short circuit or overload

Digital outputs

This register is used to indicate the output status of the digital outputs. As a result, the output with the lowest channel number is located in the LSB in each case; the bits of the channels configured as input are ignored when set.

Bit	Name	Value	Information
0	Channel 1	0	Digital output reset
		1	Digital output set
...		...	
7	Channel 8	0	Digital output reset
		1	Digital output set

7.4.2.2 X67DO9332.L12-C01

Register	Name	Bytes	Module X67DO9332.L12-C01	
Input:				
28	Actuator supply status	1	Byte	
Output:				
2	Digital outputs	1		Byte
Data bytes in DP frame			1 in	1 out

1) The register is transferred acyclically.

Actuator supply status

This register contains the state of the actuator power supply for digital outputs 1 to 8.

Data type	Values
USINT	See bit structure.

Bit	Name	Value	Information
0	Channel 1	0	Channel 01: Supply within valid range
		1	Channel 01: Short circuit or overload
...		...	
8	Channel 8	0	Channel 08: Supply within valid range
		1	Channel 08: Short circuit or overload

Digital outputs

This register is used to indicate the output status of the digital outputs. As a result, the output with the lowest channel number is located in the LSB; the bits of the outputs that are not present are ignored by the module.

Bit	Name	Value	Information
0	Channel 1	0	Digital output reset
		1	Digital output set
...		...	
7	Channel 8	0	Digital output reset
		1	Digital output set

7.4.3 Digital mixed modules

7.4.3.1 X67DM1321 (8-channel)

Register	Name	Bytes	Module					
			X67DM1321-C01		X67DM1321-C02		X67DM1321-C03	
Input:								
0	Digital inputs1 - 8	1	Byte		Byte		Byte	
30	Status of the outputs	1			Byte			
Output:								
2	Digital outputs 1 - 8	1		Byte		Byte		Byte
16	Switching between digital inputs/outputs	1		1)		1)		Byte
18	Input filter	1		1)		1)		Byte
Data bytes in DP frame			1 in	1 out	2 in	1 out	1 in	3 out

Table 7: Part 1

1) The register is transferred acyclically.

Register	Name	Bytes	Module			
			X67DM1321-C04		X67DM1321-C21[1]	
Input:						
0	Digital inputs1 - 8	1	Byte		Byte	
26	Input latch				Byte	
30	Status of the outputs	1	Byte			
Output:						
2	Digital outputs 1 - 8	1		Byte		Byte
16	Switching between digital inputs/outputs	1		Byte		2)
18	Input filter	1		Byte		2)
28	Reset input latch	1				Byte
Data bytes in DP frame			2 in	3 out	2 in	2 out

Table 8: Part 2

1) X67DM1321 firmware version ≥1.20 (supplied with revision E0 and later)
2) The register is transferred acyclically.

Register	Name	Bytes	Module							
			X67DM1321-C11[1]		X67DM1321-C12[1]		X67DM1321-C13		X67DM1321-C14	
Input:										
4	Counter 1	2	Word		Word		Word		Word	
6	Counter 2	2	Word		Word		Word		Word	
0	Digital inputs 1 - 8	1	Byte		Byte		Byte		Byte	
30	Status of the outputs	1			Byte				Byte	
Output:										
2	Digital outputs 1 - 8	1		Byte		Byte		Byte		Byte
16	Switching between digital inputs/outputs	1		2)		2)		Byte		Byte
18	Input filter	1		2)		2)		Byte		Byte
20	Counter configuration 1	1		2)		2)		Byte		Byte
22	Counter configuration 2	1		2)		2)		Byte		Byte
Data bytes in DP frame			5 in	1 out	6 in	1 out	5 in	5 out	6 in	5 out

Table 9: Part 3

1) Resetting the counters is not possible with this configuration
2) The register is transferred acyclically.

Digital inputs

This register is used to indicate the input state of digital inputs 1 to 8. As a result, the input with the lowest channel number is located in the LSB; the bits of the inputs that are not present are 0.

Bit	Name	Value	Information
0	Channel 1	0 or 1	Input state - Digital input 1
...		...	
7	Channel 8	0 or 1	Input state - Digital input 8

Status of the outputs

This register is used to indicate the status of the digital outputs.

In models **X67DM1321-C02, -C04, -C12** and **-C14**, this status information is transferred with the cyclic data; a diagnostics message is also sent to the ProfibusDP master when an error occurs.

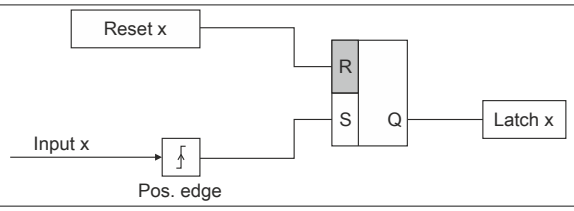
In GSD models **X67DMxxxx-Cx1** and **-Cx3** as well as **X67DM1321-C21**, this information is not provided. The models should be used in the event that this data is not required as cyclic information. However, if an error does occur then a diagnostics message will still be sent.

Bit	Name	Value	Information
0	Channel 1	0	No error
		1	Short circuit or overload
...		...	
7	Channel 8	0	No error
		1	Short circuit or overload

Input latch

Using this function, the rising edges of the input signal can be latched with a resolution of 200 µs. With the "Acknowledge - input latch" function, the input latch is either reset or prevented from latching.

It works in the same way as a dominant reset RS flip-flop.



R	S	Q	Status
0	0	x	Do not change
0	1	1	Set
1	0	0	Reset
1	1	0	Reset

Bit	Name	Value	Information
0	Channel 1	0 or 1	Input state of digital input 1 after expiration of the delay time
...		...	
7	Channel 8	0 or 1	Input state of digital input 2 after expiration of the delay time

Digital outputs

This register is used to indicate the output status of the digital outputs. As a result, the output with the lowest channel number is located in the LSB in each case; the bits of the channels configured as input are ignored when set.

Bit	Name	Value	Information
0	Channel 1	0	Digital output reset
		1	Digital output set
...		...	
7	Channel 8	0	Digital output reset
		1	Digital output set

Switching between digital inputs/outputs

This register makes it possible to configure the channels as input or output. Defines channel handling using output monitoring or filtering. Outputs are monitored but not filtered.

In models **X67DM1321-Cx3** and **-Cx4**, this register is placed in the cyclic data, thereby making it available only for configuration during operating via the I/O data instead of for the acyclic configuration.

Bit	Name	Value	Information
0	Channel 1	0	Use as an input
		1	Use as an output
...		...	
7	Channel 8	0	Use as an input
		1	Use as an output

Input filter

The filter value can be configured in steps of 100 µs. It makes sense to enter values in steps of 2, however, since the input signals are sampled every 200 µs. In models **X67DM1321-Cx3** and **-Cx4**, this register is placed in the cyclic data, thereby making it available only for configuration during operating via the I/O data instead of for the acyclic configuration.

Values	Filter
0	No software filter
2	0.2 ms
...	...
250	25 ms - Higher values are limited to this value

Reset input latch

Used to reset the corresponding channels and prevent latching. See diagram Input latch.

Bit	Name	Value	Information
0	Acknowledge latch 1	0	No influence on the latch status
		1	Resets the latch status
...		...	
7	Acknowledge latch 8	0	No influence on the latch status
		1	Resets the latch status

Counter

This register displays the results of the individual counters. Event counter or gate measurement, depending on the operating mode. Only one of the two counters can be used for gate-time measurement.

Values
0 to 65535

Counter configuration

This register can be used to configure the individual counters.

In models **X67DM1321-Cx3** and **-Cx4**, this register is placed in the cyclic data, thereby making it available only for configuration during operating via the I/O data instead of for the acyclic configuration.

Bit	Name	Value	Information
0 - 2	Counter frequency	0	48 MHz (only with gate measurement)
		1	3 MHz (only with gate measurement)
		2	187.5 kHz (only with gate measurement)
3 - 4	Reserved	0	
5	Reset counter	0	No influence on the counter
		1	Clear counter (at rising edge)
6 - 7	Type of measurement	0	Event counter measurement
		1	Gate measurement

7.4.3.2 X67DM1321 (16-channel)

Register	Name	Bytes	Module							
			X67DM ... ... 1321.L08-C02 ... 1321.L12-C02 ... 1321.L12-1-C02[2]		X67DM ... ... 1321.L08-C12[1] ... 1321.L12-C12[1] DM 1321.L12-1-C12[2]		X67DM ... ... 1321.L08-C14 ... 1321.L12-C14 ... 1321.L12-1-C14[2]		X67DM ... ... 1321.L08-C22 ... 1321.L12-C22 ... 1321.L12-1-C22[2]	
Input:										
4	Counter 1	2			Word		Word			
6	Counter 2	2			Word		Word			
0	Digital inputs 1 - 8	1	Byte		Byte		Byte		Byte	
1	Digital inputs 9 - 16	1	Byte		Byte		Byte		Byte	
26	Input latch 1 - 8	1							Byte	
27	Input latch 9 - 16	1							Byte	
30	Status of the outputs 1 - 8	1	Byte		Byte		Byte		Byte	
31	Status of the outputs 9 - 16	1	Byte		Byte		Byte		Byte	
Output:										
2	Digital outputs 1 - 8	1		Byte		Byte		Byte		Byte
3	Digital outputs 9 - 16	1		Byte		Byte		Byte		Byte
16	Switching between digital inputs/outputs 1 - 8	1		[3]		[3]		Byte		[3]
17	Switching between digital inputs/outputs 9 - 16	1		[3]		[3]		Byte		[3]
18	Input filter	1		[3]		[3]		Byte		[3]
20	Counter configuration 1	1				[3]		Byte		
22	Counter configuration 2	1				[3]		Byte		
28	Reset input latch 1 - 8	1								Byte
29	Reset input latch 9 - 16	1								Byte
Data bytes in DP frame			4 in	2 out	8 in	2 out	8 in	7 out	6 in	4 out

1) Resetting the counters is not possible with this configuration.
2) Connections for channels 1 and 2 are switched:
3) The register is transferred acyclically.

Counter

This register displays the results of the individual counters. Event counter or gate measurement, depending on the operating mode. Only one of the two counters can be used for gate-time measurement.

Values
0 to 65535

Digital inputs

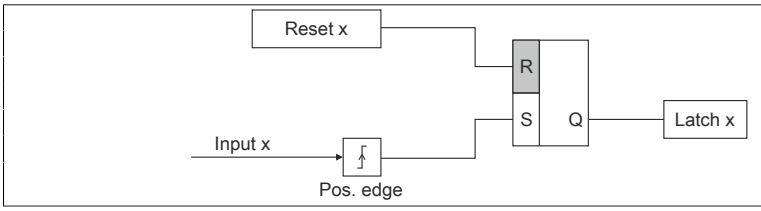
This register is used to indicate the input state of the digital inputs. As a result, the input with the lowest channel number is located in the LSB; the bits of the inputs that are not present are 0.

Bit	Name	Value	Information
0	Channel 1 or 9	0 or 1	Input state - Digital input 1 or 9
...		...	
7	Channel 8 or 16	0 or 1	Input state - Digital input 8 or 16

Input latch

Using this function, the rising edges of the input signal can be latched with a resolution of 200 µs. With the "Acknowledge - input latch" function, the input latch is either reset or prevented from latching.

It works in the same way as a dominant reset RS flip-flop.



R	S	Q	Status
0	0	x	Do not change
0	1	1	Set
1	0	0	Reset
1	1	0	Reset

Bit	Name	Value	Information
0	Channel 1 or 9	0 or 1	Input state of digital input 1 after expiration of the delay time
...		...	
7	Channel 8 or 16	0 or 1	Input state of digital input 2 after expiration of the delay time

Status of the outputs

This register is used to indicate the status of the digital outputs. However, if an error does occur then an additional diagnostics message will still be sent to the PROFIBUS DP master for all modules.

Bit	Name	Value	Information
0	Channel 1 or 9	0	No error
		1	Short circuit or overload
...		...	
7	Channel 8 or 16	0	No error
		1	Short circuit or overload

Digital outputs

This register is used to indicate the output status of the digital outputs. As a result, the output with the lowest channel number is located in the LSB in each case; the bits of the channels configured as input are ignored when set.

Bit	Name	Value	Information
0	Channel 1 or 9	0	Digital output reset
		1	Digital output set
...		...	
7	Channel 8 or 16	0	Digital output reset
		1	Digital output set

Switching between digital inputs/outputs

This register makes it possible to configure the channels as input or output. Defines channel handling using output monitoring or filtering. Outputs are monitored but not filtered.

In models **X67DM1321-C14**, this register is placed in the cyclic data, thereby making it available only for configuration during operating via the I/O data instead of for the acyclic configuration.

Bit	Name	Value	Information
0	Channel 1 or 9	0	Use as an input
		1	Use as an output
...		...	
7	Channel 8 or 16	0	Use as an input
		1	Use as an output

Input filter

The filter value can be configured in steps of 100 µs. It makes sense to enter values in steps of 2, however, since the input signals are sampled every 200 µs. In models **X67DM1321.Lxx-C14**, this register is placed in the cyclic data, thereby making it available only for configuration during operating via the I/O data instead of for the acyclic configuration.

Values	Filter
0	No software filter
2	0.2 ms
...	...
250	25 ms - Higher values are limited to this value

Counter configuration

This register can be used to configure the individual counters.

In models **X67DM1321.Lxx-C14**, this register is placed in the cyclic data, thereby making it available only for configuration during operating via the I/O data instead of for the acyclic configuration.

Bit	Name	Value	Information
0 - 2	Counter frequency	0	48 MHz (only with gate measurement)
		1	3 MHz (only with gate measurement)
		2	187.5 kHz (only with gate measurement)
3 - 4	Reserved	0	
5	Reset counter	0	No influence on the counter
		1	Clear counter (at rising edge)
6 - 7	Type of measurement	0	Event counter measurement
		1	Gate measurement

Reset input latch

Used to reset the corresponding channels and prevent latching. See diagram: Input latch.

Bit	Name	Value	Information
0	Acknowledge latch 1 or 9	0	No influence on the latch status
		1	Resets the latch status
...		...	
7	Acknowledge latch 8 or 16	0	No influence on the latch status
		1	Resets the latch status

7.4.3.3 X67DM93x1

Register	Name	Bytes	Module			
			X67DM9321-C01		X67DM9331.L12-C01	
Input:						
0	Digital inputs 1 - 8	1	Byte		Byte	
28	Status of the sensors 1 - 8	1			Byte	
30	Status of the outputs 1 - 8[2]	1				
Output:						
2	Digital outputs 1 - 8	1		Byte		Byte
16	Switching between digital inputs/outputs 1 - 8	1		[1]		[1]
18	Input filter	1		[1]		[1]
Data bytes in DP frame			1 in	1 out	2 in	1 out

1) The register is transferred acyclically.
2) Diagnostics information is automatically sent to the PROFIBUS DP master.

Digital inputs

This register is used to indicate the input state of digital inputs 1 to 8. As a result, the input with the lowest channel number is located in the LSB; the bits of the inputs that are not present are 0.

Bit	Name	Value	Information
0	Channel 1	0 or 1	Input state - Digital input 1
...		...	
7	Channel 8	0 or 1	Input state - Digital input 8

Status of the sensors

This register is used to indicate the status of the sensors.

Bit	Name	Value	Information
0	Sensor/actuator supply - Channel 1	0	Within valid range
		1	Short circuit or overload
...		...	
7	Sensor/actuator supply - Channel 8	0	Within valid range
		1	Short circuit or overload

Status of the outputs

This register is used to indicate the status of the digital outputs.

Bit	Name	Value	Information
0	Channel 1	0	No error
		1	Short circuit or overload
...		...	
7	Channel 8	0	No error
		1	Short circuit or overload

Digital outputs

This register is used to indicate the output status of the digital outputs. As a result, the output with the lowest channel number is located in the LSB in each case; the bits of the channels configured as input are ignored when set.

Bit	Name	Value	Information
0	Channel 1	0	Digital output reset
		1	Digital output set
...		...	
7	Channel 8	0	Digital output reset
		1	Digital output set

Switching between digital inputs/outputs

This register makes it possible to configure the channels as input or output. Defines channel handling using output monitoring or filtering. Outputs are monitored but not filtered.

With the **X67DM9331.L12-C01**, the register can be modified in the parameter dialog box for the I/O module and is transferred asynchronously. The counter cannot be reset with this configuration.

Bit	Name	Value	Information
0	Channel 1	0	Use as an input
		1	Use as an output
...		...	
7	Channel 8	0	Use as an input
		1	Use as an output

Input filter

The filter value can be configured in steps of 100 µs. It makes sense to enter values in steps of 2, however, since the input signals are sampled every 200 µs.

Values	Filter
0	No software filter
2	0.2 ms
...	...
250	25 ms - Higher values are limited to this value

7.4.3.4 X67DV1311

Register	Name	Bytes	Module	
			X67DV1311.L08-C02 X67DV1311.L12-C02	
Input:				
0	Digital inputs 1 - 8	1	Byte	
1	Digital inputs 9 - 16	1	Byte	
30	Status of the outputs 1 - 8	1	Byte	
31	Status of the outputs 9 - 16	1	Byte	
Output:				
2	Digital outputs 1 - 8	1		Byte
3	Digital outputs 9 - 16	1		Byte
18	Input filter	1		1)
Data bytes in DP frame			4 in	2 out

1) The register is transferred acyclically.

Digital inputs

This register is used to indicate the input state of the digital inputs. As a result, the input with the lowest channel number is located in the LSB; the bits of the inputs that are not present are 0.

Bit	Name	Value	Information
0	Channel 1 or 9	0 or 1	Input state - Digital input 1 or 9
...		...	
7	Channel 8 or 16	0 or 1	Input state - Digital input 8 or 16

Status of the outputs

This register is used to indicate the status of the digital outputs. This status information is transferred with the cyclic data; a diagnostics message is also sent to the PROFIBUS DP master when an error occurs.

Bit	Name	Value	Information
0	Channel 1	0	No error
		1	Short circuit or overload
...		...	
7	Channel 8	0	No error
		1	Short circuit or overload

Digital outputs

This register is used to indicate the output status of the digital outputs. As a result, the output with the lowest channel number is located in the LSB in each case; the bits of the channels configured as input are ignored when set.

Bit	Name	Value	Information
0	Channel 1 or 9	0	Digital output reset
		1	Digital output set
...		...	
7	Channel 8 or 16	0	Digital output reset
		1	Digital output set

Input filter

The filter value can be configured in steps of 100 µs. It makes sense to enter values in steps of 2, however, since the input signals are sampled every 200 µs.

Values	Filter
0	No software filter
2	0.2 ms
...	...
250	25 ms - Higher values are limited to this value

7.4.4 Analog input modules

7.4.4.1 X67AI1x23 / X67AI1x33

Register	Name	Bytes	Module							
			X67AI1223-C01 X67AI1323-C01 X67AI1233-C01 X67AI1333-C01		X67AI1223-C02 X67AI1323-C02 X67AI1233-C02 X67AI1333-C02		X67AI1223-C03 X67AI1323-C03 X67AI1233-C03 X67AI1333-C03		X67AI1223-C04 X67AI1323-C04 X67AI1233-C04 X67AI1333-C04	
Input:										
0	Analog input 1	2	Word		Word		Word		Word	
2	Analog input 2	2	Word		Word		Word		Word	
4	Analog input 3	2	Word		Word		Word		Word	
6	Analog input 4	2	Word		Word		Word		Word	
30	**HI:** 0 **LO:** Input status	2			Word				Word	
Output:										
16	Input filter	1		1)		1)		Byte		Byte
Data bytes in DP frame			8 in	0 out	10 in	0 out	8 in	1 out	10 in	1 out

Table 10: Part 1

1) The register can be modified in the parameter dialog box for the I/O module and is transferred acyclically.

Register	Name	Bytes	Module					
			X67AI1323-C11* X67AI1333-C11* X67AI1323-C21 X67AI1333-C21		X67AI1323-C12* X67AI1333-C12*		X67AI1323-C22	
Input:								
0	Analog input 1	2	Word		Word		Word	
2	Analog input 2	2	Word		Word		Word	
4	Analog input 3	2	Word		Word		Word	
6	Analog input 4	2	Word		Word		Word	
30	**HI:** 0 **LO:** Input status	2			Word		Word[1)]	
Output:								
16	Input filter	1		2)		2)		2)
18	Measurement range configuration	1		3)		3)		3)
20	Lower limit value	2		3)		3)		3)
22	Upper limit value	2		3)		3)		3)
Data bytes in DP frame			8 in	0 out	10 in	0 out	10 in	0 out

Table 11: Part 2

1) Acyclic diagnostics message is not sent
2) The register can be modified in the parameter dialog box for the I/O module and is transferred acyclically.
3) The register is transferred acyclically.

Module names with '*': Support with firmware version ≥ V1.43

Analog input

The analog input value is mapped in this register.

Values	Input signal
-32,768 to 32,767	**X67AI12xx:** Voltage signal -10 to 10 VDC
0 to 32,767	**X67AI13xx:** Current signal 0 to 20 mA or 4 to 20 mA

Input status

The module inputs are monitored in this register. A change in the monitoring status is actively transmitted as an error message. The diagnostics function can be individually disabled for each channel via parameter "Channel diagnose x". If an error occurs, a diagnostics message will also be sent.

In models **-C02** and **-C04**, this information is transferred with the cyclic data; the lower byte of this word register has to be evaluated.

Bit	Description	Value	Information
0 - 1	Channel 1	00	No error
		01	Lower limit value exceeded[1)]
		10	Upper limit value exceeded
		11	Open line[1)]
...		...	
6 - 7	Channel 4	00	No error
		01	Lower limit value exceeded[1)]
		10	Upper limit value exceeded
		11	Open line[1)]

1) **Only X67Ax1323:** The input value has a lower limit of 0x0. Underflow monitoring is therefore not necessary. Open line is not displayed.

Limiting the analog value

In addition to the status information, the analog value is set to the values listed below by default when an error occurs. The analog value is limited to the new values if the limit values were changed.

Error status	Digital value for error (default values)	
	X67Ax12x3	X67Ax13x3
Open line	+32767 (0x7FFF)	0x0
Upper limit value exceeded	+32767 (0x7FFF)	
Lower limit value exceeded	-32767 (0x8001)	0x0

Input filter

Filtering for all analog inputs is configured using this register. The minimum cycle time must be >500 µs.

Only X67AI1233: During shorter cycle times, the filter function is disabled regardless of the setting in this register.

If the input filter is active, then the channels are scanned in ms cycles. The time offset between the channels is 200 µs. The conversion takes place asynchronously to the network cycle.

Bit	Description	Value	Information
0 - 2	Defines the filter level	000	Filter switched off
		001	Filter level 2
		010	Filter level 4
		011	Filter level 8
		100	Filter level 16
		101	Filter level 32
		110	Filter level 64
		111	Filter level 128
3	Reserved	0	
4 - 6	Defines the input ramp limitation	000	The input value is used without limitation
		001	Limit value = 0x3FFF (16383)
		010	Limit value = 0x1FFF (8191)
		011	Limit value = 0x0FFF (4095)
		100	Limit value = 0x07FF (2047)
		101	Limit value = 0x03FF (1023)
		110	Limit value = 0x01FF (511)
		111	Limit value = 0x00FF (255)
7	Reserved	0	

Measurement range configuration

Register only exists in the X67AI1333 module.

This register allows switching of the individual inputs between 0 - 20 mA and 4 - 20 mA.

Bit	Description	Value	Information
0	Channel 1	0	Measurement range 0 to 20 mA
		1	Measurement range 4 to 20 mA
...		...	
3	Channel 4	0	Measurement range 0 to 20 mA
		1	Measurement range 4 to 20 mA
4 - 7	Reserved	-	

Lower limit value

This register can be used to configure the lower limit for analog values. If the analog value goes below the limit value, it is frozen at this value and the corresponding error status bit is set.

Values
-32,768 to 32,767

Information:

- **The default value of -32768 corresponds to the minimum default value of -10 VDC.**
- **When configured as 0 to 20 mA, this value should be set to 0.**
- **When configured as 4 to 20 mA, this value can be set to -8192 (corresponds to 0 mA) in order to display values <4 mA.**

Information:

Keep in mind that this setting applies to all channels!

Upper limit value

This register can be used to configure the upper limit for analog values. If the analog value goes above the limit value, it is frozen at this value and the corresponding error status bit is set.

Values
-32,768 to 32,767

Information:

The default value of 32767 corresponds to the maximum default value of 20 mA or +10 VDC.

Information:

Keep in mind that this setting applies to all channels!

7.4.4.2 X67AI2744

Register	Name	Bytes	Module X67AI2744-C03	
Input:				
4	Analog input Channel 1	4	Long	
8	Analog input Channel 2	4	Long	
2	**HI:** Reserved **LO:** A/D converter status	2	Word	
Output:				
16	A/D configuration Channel 1	1		Byte
17	A/D configuration Channel 2	1		Byte
Data bytes in DP frame			10 in	2 out

Analog input

This register contains the raw value determined by the A/D converter for the full-bridge strain gauge with 24-bit resolution.

Values	Information
0x007FFFFF to 0xFF800001	Valid value range
0x007FFFFF	Overrun
0xFF800001	Underflow
0xFF800000	Invalid value

Effective resolution

In principle, the effective resolution of the A/D converter is dependent on the data rate and the measurement range (see Effective resolution of the A/D converter).

The following table shows how the effective resolution (in bits), or the effective value range of the strain gauge value depend on the module configuration (data rate, measurement area).

Data rate f_{DATA} [Hz]	Measurement range ±16 mV/V		±8 mV/V		±4 mV/V		±2 mV/V	
	Bits	Range of values	Bits	Range of values	Bits	Range of values	Bits	Range of values
2.5	21.3	±1,290,000	20.8	±912,000	19.7	±425,000	18.7	±212,000
5	20.7	±851,000	20.3	±645,000	19.3	±322,000	18.3	±161,000
10	20.4	±691,000	19.9	±490,000	18.9	±244,000	17.9	±122,000
15	20.1	±562,000	19.3	±320,000	18.7	±212,000	17.7	±106,000
25	19.7	±425,000	19.2	±301,000	18.5	±185,000	17.5	±92,000
30	19.6	±397,000	19.0	±262,000	18.1	±140,000	17.1	±72,000
50	19.4	±346,000	18.8	±230,000	17.9	±122,000	16.9	±61,000
60	19.3	±320,000	18.8	±230,000	17.8	±114,000	16.8	±57,000
100	19.1	±280,000	18.5	±185,000	17.4	±86,000	16.4	±43,000
500	18.0	±130,000	17.3	±80,000	16.3	±40,000	15.3	±20,000
1000	17.2	±75,000	16.5	±46,000	15.6	±25,000	14.6	±12,000
2000	16.6	±49,600	16.1	±35,000	15.3	±20,000	14.3	±10,000
3750	16.2	±37,600	15.7	±26,600	14.7	±13,000	13.7	±6,600
7500	15.8	±28,500	15.3	±20,200	14.4	±10,800	13.4	±5,400

Table 12: Effective resolution of the strain gauge value in bits for the measurement range 2 to 16 mV/V

Data rate f_{DATA} [Hz]	Measurement range ±256 mV/V		±128 mV/V		±64 mV/V		±32 mV/V	
	Bits	Range of values	Bits	Range of values	Bits	Range of values	Bits	Range of values
2.5	23	±4,194,000	22.6	±3,179,000	22.1	±2,248,000	21.7	±1,703,000
5	22.3	±2,582,000	22.4	±2,767,000	21.9	±1,957,000	21.3	±1,291,000
10	22.3	±2,582,000	22	±2,097,000	21.6	±1,589,000	21	±1,049,000
15	22	±2,097,000	21.7	±1,703,000	21.3	±1,291,000	20.7	±852,000
25	21.7	±1,703,000	21.4	±1,384,000	21.1	±1,124,000	20.5	±741,000
30	21.8	±1,826,000	21.3	±1,291,000	20.8	±913,000	20.4	±692,000
50	21.3	±1,291,000	21.1	±1,124,000	20.4	±692,000	19.9	±489,000
60	21.3	±1,291,000	20.9	±978,000	20.5	±741,000	19.8	±456,000
100	20.9	±978,000	20.7	±852,000	20.2	±602,000	19.6	±397,000
500	20.1	±562,000	19.6	±397,000	19.1	±281,000	18.6	±199,000
1000	19	±262,000	18.6	±199,000	18.1	±140,000	17.5	±93,000
2000	18.5	±185,000	18.1	±140,000	17.8	±114,000	17	±66,000
3750	18.1	±140,000	17.8	±114,000	17.3	±81,000	16.6	±50,000
7500	17.7	±106,000	17.3	±81,000	16.9	±61,000	16.2	±38,000

Table 13: Effective resolution of the strain gauge value in bits for the measurement range 32 to 256 mV/V

Effective resolution of the A/D converter

The A/D converter for the module provides a 24-bit measurement value. However, the actual attainable noise-free resolution is always less than 24 bit. This "effective resolution" depends on the data rate and measurement range.

Example:

Because of the conversion method, a data rate of 2.5 Hz and a specified measurement area of 2 mV/V result in an effective resolution of 18.7 bits:

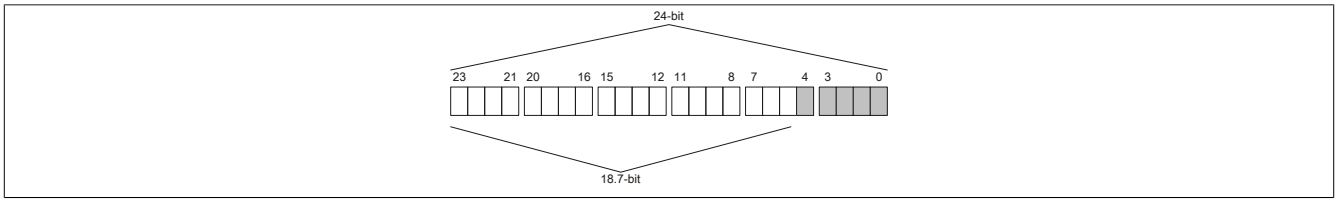


Figure 5: Example for the effective resolution of the AD converter

The low-order bits (grayed out) contain only noise instead of valid values and must therefore not be evaluated.

A/D converter status

The current state of the module is indicated in this register.

Bit	Description	Value	Information
0	A/D converter value	0	Valid A/D converter value
		1	Invalid A/D converter value
1	Line monitoring	0	OK
		1	Open line
2	Only valid in synchronous mode	0	A/D converter runs synchronous to X2X Link
		1	A/D converter does not run synchronous to X2X Link
3 - 7	Reserved	-	

A/D configuration

The sampling rate and measurement range for the A/D converter can be configured in this register.

Bit	Description	Value	Information
0 - 3	Data rate f_{DATA} (samples per second):	0000	2.5
		0001	5
		0010	10
		0011	15
		0100	25
		0101	30
		0110	50
		0111	60
		1000	100
		1001	500
		1010	1000
		1011	2000
		1100	3750
		1101	7500
		1110	Synchronous mode[1)]
		1111	Reserved
4 - 5	Standard measurement range (bit 6 = 0)	00	16 mV/V
		01	8 mV/V
		10	4 mV/V
		11	2 mV/V
	Extended measurement range (bit 6 = 1)[2)]	00	256 mV/V
		01	128 mV/V
		10	64 mV/V
		11	32 mV/V
6	Measurement range	0	Standard measurement range (2 to 16 mV/V)
		1	Extended measurement range (32 to 256 mV/V)[2)]
7	Reserved	0	(must be 0)

1) A/D converter is operated synchronously with X2X Link if possible; beginning with firmware 2
2) Starting with Firmware Version 4

7.4.4.3 X67AI4850

Register	Name	Bytes	Module X67AI4850	
Input:				
0	Analog input 1	2	Word	
2	Analog input 2	2	Word	
4	Analog input 3	2	Word	
6	Analog input 4	2	Word	
30	**HI:** 0 **LO:** Input status	2	Word	
Data bytes in DP frame			10 in	0 out

Analog input

These registers show the input voltage of the potentiometers.

Values	Input signal
0 to 32,757	Input voltage U_{pot} = 0 to 4.5 V.

Input status

The module inputs are monitored in this register. A change in the monitoring status is actively transmitted as an error message. The diagnostics function can be individually disabled for each channel via parameter "Channel diagnose x". If an error occurs, a diagnostics message will also be sent.

Bit	Description	Value	Information
0 - 1	Channel 1	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
...		...	
6 - 7	Channel 4	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line

Limiting the analog value

In addition to the status info, the error type also sets the respective analog value as follows:

Error status	Digital value for error
Open connection on Upot	0 (0x0000)
Open GND circuit	+32767 (0x7FFF)
Open line on slider	+32767 (0x7FFF)

7.4.5 Analog output modules

7.4.5.1 X67AO1x23

Register	Name	Bytes	Module X67AO1223-C01 X67AO1323-C01	
Output:				
0	Analog output 1	2		Word
2	Analog output 2	2		Word
4	Analog output 3	2		Word
6	Analog output 4	2		Word
Data bytes in DP frame			0 in	8 out

Analog output

These registers provide the standardized output values. Once a permitted value is received the module outputs the respective current or voltage.

Values	Information
-32,768 to 32,767	Voltage signal -10 to 10 VDC
0 to 32,767	Current signal 0 to 20 mA

7.4.6 Analog mixed modules

7.4.6.1 X67AM1x23

Register	Name	Bytes	Module							
			X67AM1223-C01 X67AM1323-C01		X67AM1223-C02 X67AM1323-C02		X67AM1223-C03 X67AM1323-C03		X67AM1223-C04 X67AM1323-C04	
Input:										
0	Analog input 1	2	Word		Word		Word		Word	
2	Analog input 2	2	Word		Word		Word		Word	
30	**HI:** 0 **LO:** Input status	2			Word				Word	
Output:										
8	Analog output 1	2		Word		Word		Word		Word
10	Analog output 2	2		Word		Word		Word		Word
16	**HI:** 0 **LO:** Input filter	2		1)				Word		Word
Data bytes in DP frame			4 in	4 out	6 in	4 out	4 in	6 out	6 in	6 out

1) The register can be modified in the parameter dialog box for the I/O module and is transferred acyclically.

Analog input

The analog input value is mapped in this register.

Values	Input signal
-32,768 to 32,767	**X67AI1223:** Voltage signal -10 to 10 VDC
0 to 32,767	**X67AI1323:** Current signal 0 to 20 mA

Input status

The module inputs are monitored in this register. A change in the monitoring status is actively transmitted as an error message. The diagnostics function can be individually disabled for each channel via parameter "Channel diagnose x". If an error occurs, a diagnostics message will also be sent.

In models **-C02** and **-C04**, this information is transferred with the cyclic data; the lower byte of this word register has to be evaluated.

Bit	Description	Value	Information
0 - 1	Channel 1	00	No error
		01	Lower limit value exceeded1)
		10	Upper limit value exceeded
		11	Open line1)
...		...	
6 - 7	Channel 4	00	No error
		01	Lower limit value exceeded1)
		10	Upper limit value exceeded
		11	Open line1)

1) **Only X67Ax1323:** The input value has a lower limit of 0x0. Underflow monitoring is therefore not necessary. Open line is not displayed.

Limiting the analog value

In addition to the status information, the analog value is set to the values listed below by default when an error occurs. The analog value is limited to the new values if the limit values were changed.

Error status	Digital value for error (default values)	
	X67Ax12x3	X67Ax13x3
Open line	+32767 (0x7FFF)	0x0
Upper limit value exceeded	+32767 (0x7FFF)	
Lower limit value exceeded	-32767 (0x8001)	0x0

Analog output

These registers provide the standardized output values. Once a permitted value is received the module outputs the respective current or voltage.

Values	Information
-32,768 to 32,767	Voltage signal -10 to 10 VDC
0 to 32,767	Current signal 0 to 20 mA

Input filter

Filtering for all analog inputs is configured using this register. The minimum cycle time must be >500 µs.

If the input filter is active, then the channels are scanned in ms cycles. The time offset between the channels is 500 µs. The conversion takes place asynchronously to the network cycle.

Bit	Description	Value	Information
0 - 2	Defines the filter level	000	Filter switched off
		001	Filter level 2
		010	Filter level 4
		011	Filter level 8
		100	Filter level 16
		101	Filter level 32
		110	Filter level 64
		111	Filter level 128
3	Reserved	0	
4 - 6	Defines the input ramp limitation	000	The input value is used without limitation
		001	Limit value = 0x3FFF (16383)
		010	Limit value = 0x1FFF (8191)
		011	Limit value = 0x0FFF (4095)
		100	Limit value = 0x07FF (2047)
		101	Limit value = 0x03FF (1023)
		110	Limit value = 0x01FF (511)
		111	Limit value = 0x00FF (255)
7	Reserved	0	

7.4.7 Communication modules

7.4.7.1 X67IF1121-1

Register	Name	Bytes	Module X67IF1121-1	
Input:				
135	Digital inputs	1	Byte	
133	Status of digital outputs	1	Byte	
0	IF1 Input sequence	1	Byte	
1	IF1 RxBytes 1	1	Byte	
...	...	...	...	
7	IF1 RxBytes 7	1	Byte	
64	IF2 Input sequence	1	Byte	
65	IF2 RxBytes 1	1	Byte	
...	...	...	...	
71	IF2 RxBytes 7	1	Byte	
Output:				
129	Digital outputs	1		Byte
32	IF1 Output sequence	1		Byte
33	IF1 TxBytes 1	1		Byte
...	...	...		...
39	IF1 TxBytes 7	1		Byte
96	IF2 Output sequence	1		Byte
97	IF2 TxBytes 1	1		Byte
...	...	...		...
103	IF2 TxBytes 7	1		Byte
1294	Input filter	1		1)
20	IF1 Configuration - Interfaces	1		1)
28	IF1 Setting the baud rate	1		1)
52	IF2 Configuration - Interfaces	1		1)
60	IF2 Setting the baud rate	1		1)
	Data bytes in DP frame		18 in	17 out

1) The register is transferred acyclically.

Support with firmware version ≥ V1.43

Digital inputs

This register indicates the input state of digital inputs 1 to 4.

Bit	Name	Value	Information
0	Channel 1	0 or 1	Input status of digital input 1
...		...	
3	Channel 4	0 or 1	Input status of digital input 4

Status of digital outputs

This register is used to indicate the status of digital outputs 3 and 4.

Bit	Description	Value	Information
0 - 1	Reserved	-	
2	Channel 3	0	Channel 03: No error
		1	Channel 03: Short circuit or overload
3	Channel 4	0	Channel 04: No error
		1	Channel 04: Short circuit or overload
4 - 7	Reserved	-	

Input sequence

This register contains information about the communication status of the module. It is written by the module and should only be read by the CPU.

Bit	Name	Value	Information
0 - 2	Input sequence counter	0 to 7	Counter for sequences issued in the input direction
3	InputSynchronous	0	Not ready (disabled)
		1	Ready (enabled)
4 - 6	Acknowledged output sequence	0 to 7	Mirrors the output sequence counter value
7	OutputSynchronous	0	Not ready (disabled)
		1	Ready (enabled)

Input sequence counter

The input sequence counter is a continuous counter of sequences that have been issued by the module. The module uses the input sequence counter to direct the CPU to accept a sequence (the input direction must be synchronized when this happens).

InputSynchronous

The module uses this to attempt to synchronize the input channel.

Acknowledged output sequence

This value is used for acknowledgment. The value of the output sequence counter is mirrored if the module has received a sequence successfully.

OutputSynchronous

This bit acknowledges the synchronization of the output channel for the CPU. This indicates that the module is ready to receive data.

Information:

It is still possible to split up a message into several segments, however. If this option is used and messages with more than 63 bytes occur, for example, then messages can still be split up among several segments.

RxBytes

Conversion time
Channel 0x sampling rate

The Tx and Rx bytes are cyclic registers used to transport the payload data and the necessary control bytes. The number of active Tx and Rx bytes is taken from the configuration of the OutputMTU and InputMTU registers, respectively.
In the user program, only the Tx and Rx bytes from the CPU can be used. The corresponding counterparts are located in the module and are not accessible to the user. For this reason, names were chosen from the CPU point of view.

- "T" - "Transmit" →CPU *transmits* data to the module.
- "R" - "Receive" →CPU *receives* data from the module.

Values
0 to 65,535

Digital outputs

This register is used to store the switching state of digital outputs 3 to 4.

Bit	Name	Value	Information
0 - 1	Reserved	-	
2	Channel 3	0	Digital output 03 reset
		1	Digital output 03 set
3	Channel 4	0	Digital output 04 reset
		1	Digital output 04 set
4 - 7	Reserved	-	

Output sequence

Values
0 to 65,535

This register contains information about the communication status of the CPU. It is written by the CPU and read by the module.

Bit	Name	Value	Information
0 - 2	Output sequence counter	0 to 7	Counter for sequences issued in the output direction
3	OutputSynchronous	0	Output direction disabled
		1	Output direction enabled
4 - 6	Acknowledged input sequence	0 to 7	Mirrors the input sequence counter value
7	InputSynchronous	0	Input direction not ready (disabled)
		1	Input direction ready (enabled)

Output sequence counter

The output sequence counter is a continuous counter of sequences that have been issued by the CPU. The CPU uses the output sequence counter to direct the module to accept a sequence (the output direction must be synchronized when this happens).

OutputSynchronous

The CPU uses this bit to attempt to synchronize the output channel.

Acknowledged input sequence

This value is used for acknowledgment. The value of the input sequence counter is mirrored if the CPU has received a sequence successfully.

InputSynchronous

This bit acknowledges the synchronization of the input channel for the module. This indicates that the CPU is ready to receive data.

TxBytes

See RxBytes.

Input filter

This register can be used to specify the filter value for all digital inputs.

The filter value can be configured in steps of 100 µs. It makes sense to enter values in steps of 2, however, since the input signals are sampled every 200 µs.

Data type	Value	Filter
USINT	0	No software filter (default value)
	2	0.2 ms
	...	...
	250	25 ms - Higher values are limited to this value

Configuration - Interfaces

These registers are used to configure the interfaces. Only the corresponding interface values are permitted to be used for each register.

- IF1CfgPhy configures RS232 interface
- IF2CfgPhy configures RS422/485 interface

After all other configuration registers have been written, the last write command must enable the interface. If parameters need to be changed, the interface must first be disabled.

Bit	Description	Value	Information
0 - 7	Parity bit configuration[1)]	48	"0" - (low) bit is always 0
		49	"1" - (high) bit is always 1
		69	"E" - (even) even parity (default)
		78	"N" - (no) no bit
		79	"O" - (odd) odd parity
8 - 15	Number of stop bits	2	1 stop bit (default)
		4	2 stop bits
16 - 23	Number of data bits per character	7	7 data bits
		8	8 data bits (default)
24 - 31	Interface mode	0	Interface disabled (default)
		2	RS232 interface active
		4	RS422 interface active[2)]
		5	RS422 interface active as bus[3)]
		6	RS485 interface active with echo
		7	RS485 interface active without echo

1) ASCII-encoded decimal values
2) Connection between 2 stations
3) Connections between multiple stations possible. Transmit lines connected as with RS485 tri-state.

Setting the baud rate

This register sets the baud rate of the interface in bit/s.

Data type	Value	Function
UDINT	1200	1.2 kbaud
	2400	2.4 kbaud
	4800	4.8 kbaud
	9600	9.6 kbaud
	19200	19.2 kbaud
	38400	38.4 kbaud
	57600	57.6 kbaud
	115200	115.2 kbaud

7.4.8 Motor modules

7.4.8.1 X67MM2436

Register	Name	Bytes	Module X67MM2436-C02	
Input:				
0	Counters 1	2	Word	
2	Counters 2	2	Word	
6	Counter latch 1	2	Word	
8	Counter latch 2	2	Word	
10	**HI:** 0 **LO:** Input / Limit switch state	2	Word	
22	usSinceTrigger	2	Word	
24	**HI:** 0 **LO:** Status information	2	Word	
32	**HI:** 0 **LO:** Error state	2	Word	
Output:				
4	Counter configuration	1		1)
12	PWM period duration	2		Word
14	PWM pulse width or current 1	2		Word
16	PWM pulse width or current 2	2		Word
18	Dither amplitude	1		1)
20	Dither frequency	1		1)
26	**HI:** 0 **LO:** Counter latch / Trigger configuration	2		Word
30	Module configuration	1		1)
34	**HI:** 0 **LO:** Error acknowledgment	2		Word
Data bytes in DP frame			16 in	10 out

1) The register can be modified in the parameter dialog box for the I/O module and is transferred acyclically.

Counters

These registers indicate the status of counters 1 and 2. The configuration of the counters is described in section Counter configuration.

The following counter types or measurements can be configured (starting with firmware version 8):

- AB counters
- ABR counters ("single" or "continuous" referencing)
- Event counters
- Period measurement
- Gate measurement

Assignments of digital inputs

Counter function	Counter number	A	B	R	Counter input	Period duration and gate measurement signal	External Measuring frequency
Incremental encoders	1	DI 1	DI 2	DI 3			
	2	DI 4	DI 5	DI 6			
Event counters	1				DI 1		
	2				DI 4		
Period duration and gate measurement	1					DI 1	DI 3
	2					DI 4	DI 6

Counter latch

The current state of the counter is saved in the respective register when the latch event occurs.

Values
0 to 65,535

Input / Limit switch state

This register contains the state of the inputs and limit switches.

Bit	Description	Value	Information
0	Input channel 1	x	Input status - Channel 1
...		...	
5	Input channel 6	x	Input status - Channel 6
6	Limit switch 1	0	Limit switch 1 has not been triggered.
		1	Limit switch 1 has been triggered.
7	Limit switch 2	0	Limit switch 2 has not been triggered.
		1	Limit switch 2 has been triggered.

The following applies to bits 6 and 7:

The bit is set to "1" as soon as an edge occurs on logical input 3 or 6 when the limit switch is enabled (see "Module configuration"). Bits 6 and 7 are set to 0 again when the limit switch is disabled or after acknowledgment via register "Error acknowledgment".

usSinceTrigger

This register indicates the time (in microseconds) that has passed since the trigger event occurred (see Counter latch / Trigger configuration).

Values
0 to 65,535

Status information

This register shows the latch, trigger and overload status of the individual counters.

Bit	Description	Value	Information
0	Latch status 1	0	The latch function for counter 1 has been enabled (see Counter latch / Trigger configuration). Register Counter latch 1 does not contain a valid value.
		1	Counter 1 has been latched.
1	Latch executed 1	x	State changes each time counter 1 is successfully latched (reset value = 0)
2	Latch status 2	0	The latch function for counter 2 has been enabled (see Counter latch / Trigger configuration). Register Counter latch 2 does not contain a valid value.
		1	Counter 2 has been latched.
3	Latch executed 2	x	State changes each time counter 2 is successfully latched (reset value = 0)
4	Trigger	x	Trigger input state (level)
5	Reserved	-	
6[1)]	Valid range for counter 1	0	Period duration and gate measurement are within the valid range (0x0 - 0xFFFF); the bit is only valid if overflow detection is enabled (bit 2 = 1 in register Error acknowledgment).
		1	Overflow during period duration or gate measurement (reset with bit 2 = 0 in register Error acknowledgment)
7[1)]	Valid range for counter 2	0	Period duration and gate measurement are within the valid range (0x0 - 0xFFFF); the bit is only valid if overflow detection is enabled (bit 3 = 1 in register Error acknowledgment).
		1	Overflow during period duration or gate measurement (reset with bit 3 = 0 in register Error acknowledgment)

1) Supported starting with firmware version 8

Error state

If an error is detected, the corresponding error bit remains set until the error is acknowledged (see Error acknowledgment).

Bit	Description	Value	Information
0	Undervoltage	0	No error
		1	Lower limit of I/O power supply < 15 V
1	Overvoltage	0	No error
		1	Upper limit of I/O power supply > 50 V
2	Overtemperature	0	No error
		1	Overtemperature
3	Reserved	-	
4	Open load error 1	0	No error
		1	Open load - Output 1
5	Overcurrent 1	0	No error
		1	Overcurrent - Output 1
6	Open load error 2	0	No error
		1	Open load - Output 2
7	Overcurrent 2	0	No error
		1	Overcurrent - Output 2

An **overcurrent error** is registered if one of the following conditions is met:

- ≥5 A flow from a PWM output for at least 2 seconds
- ≥8 A flow for 3 consecutive PWM cycles.

In either case, the affected PWM output is disabled by the firmware (i.e. the pins on the PWM output are short circuited). A PWM output disabled in this way can only be put into service again by the user after error acknowledgment (see Error acknowledgment).

An **open load error** is only registered in current control mode (see Module configuration) if the set current is not reached. In some cases this can be caused by an open circuit, although usually the impedance of the load is too high.

Counter configuration

The counters can be configured together in this register.

Bit	Description	Value	Information
0 - 1	Latch counter 1	00	Counter 1 latch unconditional
		01	Counter 1 latch on positive edge of input E3 (R pulse)
		10	Counter 1 latch on negative edge of input E3 (R pulse)
		11	Reserved
2	Latch mode 1	0	One-time
		1	Continuous[1)]
3	Latch mode 2	0	One-time
		1	Continuous[1)]
4 - 5	Latch counter 2	00	Counter 2 latch unconditional
		01	Counter 2 latch on positive edge of input E6 (R pulse)
		10	Counter 2 latch on negative edge of input E6 (R pulse)
		11	Reserved
6 - 7	Trigger input	00	No trigger input
		01	E3 is used as a trigger input.
		10	E6 is used as a trigger input.
		11	Reserved

1) Supported starting with firmware version 8

Bits 0 to 1 or 4 to 5 are used to configure the time for counters 1 and 2 at which the latch event occurs for applying the counter value to register "Counter latch". This setting is only relevant if the latch function has been enabled in the configuration register (see Counter latch / Trigger configuration).

Setting "Counter 1/2 latch unconditional" means that the latch event is triggered when the latch function is enabled.

The following function is only supported with firmware V8 or later:

Bit	Description	Value	Information
0 - 2	Type of counter	000	ABR counter (4x evaluation)
		001	Event counters
		010	Period measurement
		011	Gate measurement
		100	AB counter (4x evaluation)
		101 to 111	No counter (counter disabled and hidden in I/O map)
3	Counter start	0	Starts the counter on a rising edge
		1	Starts the counter on a falling edge
4 - 5	Counter frequency	00	4 MHz (gate and period measurement)
		01	External (gate and period measurement)
		10	31.25 kHz (gate and period measurement)
		11	Reserved
6 - 7	Reserved	-	

PWM period duration

The period duration can be set from 20 µs (50 kHz) to 65535 µs (15 Hz) in this register.

Values	Information
20 to 65535	Time in microseconds

PWM pulse width or current

The PWM pulse width (PWM mode) or current setting (in current mode) is specified here based on the setting in the module configuration register. The output polarity is reversed if the value is negative.

PWM mode

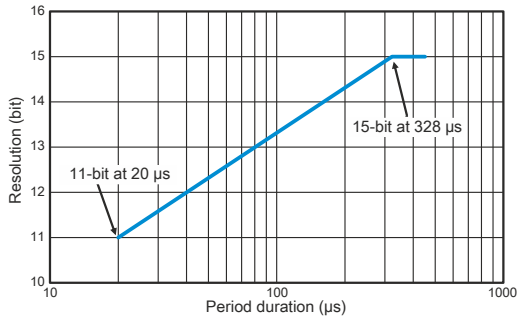
Value	Output +	Output -
32767	High	Low
16384	PWM 50/50	Low
0	Low	Low
-16384	Low	PWM 50/50
-32767	Low	High

Current mode

Value	Current mode
+19661 to +32767	+3 to 5 A (max. 2 s)
+19,960	+3 A
0	0 A
-19,960	-3 A
-19,661 to -32,767	-3 to -5 A (max. 2 s)

Resolution/Derating

As mentioned earlier in the technical data, the PWM has 15-bit resolution (+ sign). This value is derated for a period duration of less than 328 µs because of the minimal PWM timing resolution (10 ns) (see following diagram). With the minimum PWM period duration of 20 µs, the PWM has 11-bit resolution (+ sign):



Dither amplitude

The amplitude value or the pulse width can be set in this register.
0 to 255 corresponds with an amplitude value from 0 to 25.5% of the maximum current or the maximum pulse width of 32767.

Values	Information
0 to 255	Amplitude value or pulse width

Dither frequency

The frequency can be specified in steps of 2 Hz in this register.

Values	Information
0 to 255	Corresponds to 0 to 510 Hz

Counter latch / Trigger configuration

This register is used to configure the latch function and the trigger edge for the individual counters.

Bit	Description	Value	Information
0	Latch function 1	0	Disables the latch function for counter 1 on the negative edge of this bit
		1	Disables the latch function for counter 1 on the positive edge of this bit
1	Latch function 2	0	Disables the latch function for counter 2 on the negative edge of this bit
		1	Disables the latch function for counter 2 on the positive edge of this bit
2 - 3	Reserved	-	
4	Setting the trigger edge	0	Triggers a trigger event on the positive edge of the trigger input
		1	Triggers a trigger event on the negative edge of the trigger input
5	Activate trigger	x	Enables the trigger when this bit is changed (0 to 1, or 1 to 0)
6 - 7	Reserved	-	

Trigger function procedure (bits 4 and 5):

- Bit 4 is used to select the desired trigger edge.
- Changing the state of bit 5 enables the trigger function and clears register "usSinceTrigger" (microsecond counter).
- Microsecond counter usSinceTrigger is started when the trigger event occurs.
- Counter usSinceTrigger cannot overflow! This means that the counter is stopped at 2^{16}-1 and retains this value until the trigger function is enabled again.
- The trigger function can be **re-enabled** by changing the state of bit 5, regardless of whether a trigger event has occurred or if usSinceTrigger has reached the maximum value.

The **limit switch function** serves to quickly shut off the PWM outputs when a limit position is reached:

- The limit switches are enabled in the configuration register (see Module configuration). This is also where the input E3/E6 edge is selected for triggering a limit switch.
- The respective PWM output 1 or 2 will be disabled now as soon as the configured trigger edge occurs on the input E3/E6. It remains disabled until the limit switch is disabled or until the error is acknowledged (see Error acknowledgment).

Module configuration

The output control for each motor and the limit switch behavior can be configured in this register.

Bit	Description	Value	Information
0	Output 1	0	PWM control
		1	Current control
1	Output 2	0	PWM control
		1	Current control
2 - 3	Limit switch 1	00	Disabled
		01	Trigger edge for limit switch 1: Positive edge on E3
		10	Trigger edge for limit switch 1: Negative edge on E3
		11	Reserved (limit switch 1 disabled)
4 - 5	Limit switch 2	00	Disabled
		01	Trigger edge for limit switch 2: Positive edge on E6
		10	Trigger edge for limit switch 2: Negative edge on E6
		11	Reserved (limit switch 2 disabled)
6 - 7	Reserved	-	

Error acknowledgment

Errors can be acknowledged in this register; overflow detection, counters and dither can also be enabled or disabled in this register.

Bit	Description	Value	Information
0	Acknowledge error 1	0	No effect
		1	Error acknowledgment on output 1 (overcurrent, open load, limit switch)
1	Acknowledge error 2	0	No effect
		1	Error acknowledgment on output 2 (overcurrent, open load, limit switch)
2[1)]	Overflow detection 1	0	Overflow detection disabled. Bit 6 in the counter status register is reset.
		1	Overflow detection enabled.
3[1)]	Overflow detection 1	0	Overflow detection disabled. Bit 7 in the counter status register is reset.
		1	Overflow detection enabled.
4[1)]	Counter 1	0	Enabled
		1	The counter is set to 0 and disabled. If counter 1 is configured as an ABR counter, then counter latch 1 is set to 0.
5[1)]	Counter 2	0	Enabled
		1	The counter is set to 0 and disabled. If counter 2 is configured as an ABR counter, then counter latch 2 is set to 0.
6	Dither 1	0	Dither is enabled. The frequency and amplitude must be greater than 0.
		1	Dither is disabled.
7	Dither 2	0	Dither is enabled. The frequency and amplitude must be greater than 0.
		1	Dither is disabled.

1) Supported starting with firmware version 8

7.4.8.2 X67SM2436 / X67SM4320

Register	Name	Bytes	Module			
			X67SM2436*1) X67SM2436-C05		X67SM4320*1) X67SM4320-C05	
Input:						
0	Current position 1	4	Long		Long	
4	Status 1	2	Word		Word	
6	**HI:** 0 **LO:** Digital inputs	2	Word			
8	Current position 2	4	Long		Long	
12	Status 2	2	Word		Word	
16	Current position 3	4			Long	
20	Status 3	2			Word	
24	Current position 4	4			Long	
28	Status 4	2			Word	
Output:						
0	Position/speed 1	4		Long		Long
4	Control 1	2		Word		Word
6	**HI:** 0 **LO:** Mode 1	2		Word		Word
8	Position/speed 2	4		Long		Long
12	Control 2	2		Word		Word
14	**HI:** 0 **LO:** Mode 2	2		Word		Word
16	Position/speed 3	4				Long
20	Control 3	2				Word
22	**HI:** 0 **LO:** Mode 3	2				Word
24	Position/speed 4	4				Long
28	Control 4	2				Word
30	**HI:** 0 **LO:** Mode 4	2				Word
Data bytes in DP frame			14 in	20 out	24 in	32 out

1) The configuration registers (see "Ramp model" section in module description) can be modified in the parameter dialog box for the I/O module and are transferred asynchronously.

Module names with '*': Support with firmware version ≥ V1.43

Current position

This cyclic register contains the current position.

Default: Value of the internal position counter, can be changed to ABR counter

Values
-2,147,483,648 to 2,147,483,647

Status

The bits in this register reflect the state of the state machine.

Bit	Description	Value	Information
0	Ready to switch on	x	
1	Switched on	x	
2	Operation enabled	x	
3	Fault (error bit)	x	
4	Voltage enabled	x	
5	Quick stop	x	
6	Switch on disabled	x	
7	Warning	x	
8	Reserved	0	
9	Remote	1	Always 1 because there is no local mode for the SM module
10	Target reached	x	
11	Internal limit active	0	No limit violation
		1	Internal limit is active (upper/lower software limit violated)
12	Mode-specific	x	
13 - 15	Reserved	0	

Digital inputs

Register only exists in the X67SM2436 module.

This register indicates the logical states of digital inputs.

Bit	Description	Value	Information
0	Digital input 1	0 or 1	Input state - Digital input 1
...		...	
3	Digital input 4	0 or 1	Input state - Digital input 4
4 - 15	Reserved	0	

Position/speed

This register is used to set position or speed, depending on the operating mode.

- Position mode (see Mode): Cyclic setting of the position setpoint in microsteps. In this mode, one micro-step is always 1/256 full-step.
- Speed mode (see Mode): In this mode, this register is used as a signed speed setpoint.

Values
-2,147,483,648 to 2,147,483,647

Control

This register can be used to issue commands based on the module's state.

Bit	Description	Value	Information
0	Switch on	x	
1	Enable voltage	x	
2	Quick stop	x	
3	Enable operation	x	
4 - 6	Mode-specific	x	
7	Fault reset	x	
8	Halt[1)]	x	
9 - 10	Reserved	0	
11	Motor ID trigger	0	No effect
		1	Rising edge: Motor ID trigger[2)]
12	Warning reset	0	No effect
		1	Rising edge: Reset warnings
13	Undercurrent detection	0	Disable current error detection (default)
		1	Enable current error detection
14	ABR counter sync/async	0	Default: • Internal position counter, cyclic • ABR counter, acyclic
		1	• Internal position counter, acyclic • ABR counter, cyclic
15	Stall detection	0	Disable stall detection (default)
		1	Enable stall detection

1) The "Halt" bit is only evaluated when the extended control word is enabled.
2) This bit can be used to trigger a measurement of the motor ID. Keep in mind that the application must ensure that the conditions are fulfilled for this.

Mode

Values	Information
0	No mode selected
1	The position setpoint is specified as set in the Position/speed register. The motor is then moved to this new position. This is done with a ramp function that accounts for the defined maximum speed and acceleration values. The position setpoint can also be changed during an active positioning procedure. The position setpoint is specified in microsteps (1/256 of a full step). The position setpoint will be applied as soon as it differs from the current position. The new position is then moved to.
2	The value in the Position/speedregister is interpreted as the speed setpoint (microsteps/cycle). Observing the maximum permissible acceleration, the motor moves with a ramp to the desired speed setpoint and maintains this speed until a new speed setpoint is specified. Values are allowed within the range -65535 to 65535. When a value is entered outside of this range, it is readjusted to these limits.

Information:

For all modes: The "Target reached" bit is set in the Status register when the current action is finished (i.e. when the position or speed is reached, depending on the mode).

A new position or speed can be specified even before the current action is finished.

7.4.9 Other modules

7.4.9.1 X67UM1352

Register	Name	Bytes	Module X67UM1352-C02	
Input:				
16	Strain gauge value	4	Long	
0	Digital inputs 1 - 4	1	Byte	
28	ADC status	1	Byte	
30	Status[1)]	1		
Output:				
2	Digital outputs 1-2	1		Byte
26	ADC configuration	1		[2)]
Data bytes in DP frame			6 in	1 out

1) Diagnostics information is automatically sent to the PROFIBUS DP master.
2) The register can be modified in the parameter dialog box for the I/O module and is transferred acyclically.

Strain gauge value

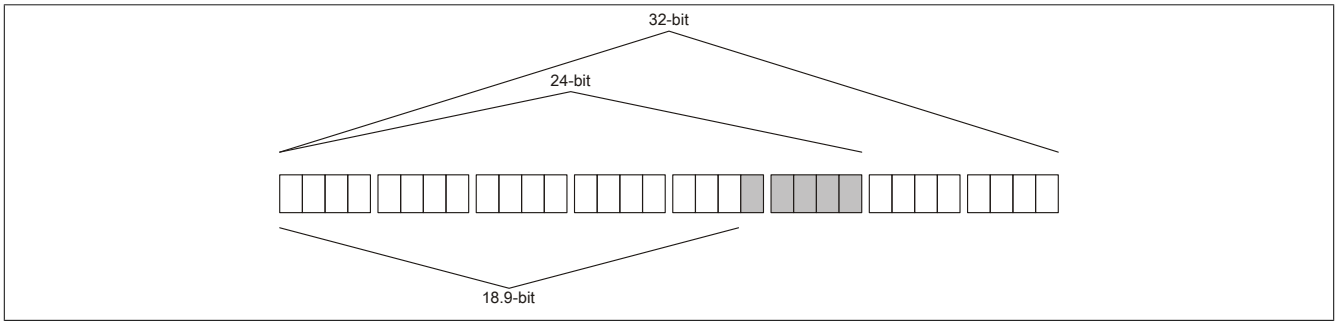
This register contains the raw value determined by the A/D converter for the full-bridge strain gauge with 24-bit resolution.

Range of values	
Valid value range	0x7FFF FFFF to 0x8000 0001 2,147,483,647 to -2,147,483,647 1 LSB = 0x0000 0100
Overrun	0x7FFF FFFF
Underflow	0x8000 0000
Invalid value	0x8000 0000

Resolution in bits

Through the sigma-delta conversion of the analog signals on the module, there is, in principal, an effective resolution of the displayed value. This means that even if the A/D converter on the module always outputs a 24-bit value, then the attainable resolution according to calculations is always smaller than the 24-bit converter resolution (see following example). The effective resolution depends on the data rate and measurement range (see section ADC configuration).

Because of the conversion method, a data rate of 10 Hz and a specified measurement area of 15.625 mV/V result in an effective resolution of 18.9 bits:



The amount of information in the low-order bits (marked in gray) can only be used to a certain extent and is subject to heavy disturbances.

The following table shows how the effective resolution (in bits), or the effective value range of the strain gauge value depend on the module configuration (data rate, measurement area).

Data rate (Hz)	Gain / Resolution							
	1 ±125 mV/V		2 ±62.500 mV/V		4 ±31.250 mV/V		8 ±15.625 mV/V	
	Bits	Range of values	Bits	Range of values	Bits	Range of values	Bits	Range of values
10	21.0	±1,000,000	20.4	±691,800	19.9	±490,000	18.9	±244,000
50	19.9	±490,000	19.4	±346,000	18.8	±230,000	17.9	±122,000
60	19.8	±450,000	19.3	±320,000	18.8	±230,000	17.8	±114,000
100	19.6	±297,000	19.1	±280,000	18.5	±185,000	17.4	±86,000
500	18.6	±200,000	18.0	±130,000	17.3	±80,000	16.3	±40,000
1000	17.5	±92,000	17.2	±75,000	16.5	±46,000	15.6	±25,000
2000	17.0	±65,500	16.6	±49,600	16.1	±35,000	15.3	±20,000
3750	16.6	±49,600	16.2	±37,600	15.7	±26,600	14.7	±13,000

Resolution for 2 to 8 mV/V sensors

The setting 16 mV/V should be used for 2 to 8 mV/V sensors. This now results in the following resolution:

Data rate (Hz)	Gain / Resolution					
	8		8		8	
	±1.953 mV/V		±3.906 mV/V		±7.8125 mV/V	
	Bits	Range of values	Bits	Range of values	Bits	Range of values
10	15.9	±30,500	16.9	±61,100	17.9	±122,000
50	14.9	±15,300	15.9	±30,500	16.9	±61,100
60	14.8	±14,300	15.8	±28,400	16.8	±57,000
100	14.4	±10,800	15.4	±21,600	16.4	±43,200
500	13.3	±5,000	14.3	±10,080	15.3	±20,100
1000	12.6	±3,100	13.6	±6,200	14.6	±12,400
2000	12.3	±2,500	13.3	±5,000	14.3	±10,000
3750	11.7	±1,660	12.7	±3,300	13.7	±6,600

Digital inputs

This register is used to indicate the input state of the digital inputs. As a result, the input with the lowest channel number is located in the LSB; the bits of the inputs that are not present are 0.

Bit	Name	Value	Information
0	Channel 1	0 or 1	Input state - Digital input
...		...	
3	Channel 4	0 or 1	Input state - Digital input
4 - 7	Reserved	-	

ADC status

This register is used to indicate the status of the A/D converter.

Bit	Name	Value	Information
0	Converter status	0	No error
		1	Open connection measuring bridge
1 - 7	Reserved	-	

Status

This register is used to indicate the status of the digital outputs.

Bit	Name	Value	Information
0	Channel 1	0	No error
		1	Error digital output 1
1	Channel 2	0	No error
		1	Error digital output 2
2 - 7	Reserved	-	

Digital outputs

This register is used to indicate the output status of the digital outputs. As a result, the output with the lowest channel number is located in the LSB in each case; the bits of the channels configured as input are ignored when set.

Bit	Name	Value	Information
0	Channel 1	0	Digital output reset
		1	Digital output set
1	Channel 2	0	Digital output reset
		1	Digital output set
2 - 7	Reserved	-	

ADC configuration

This register can be used to configure the gain and sampling rate for the input signal.

Bit	Name	Value	Information
0 - 1	Gain	00	1x
		01	2x
		10	4x
		11	8x
2 - 4	Sampling rate	000	10 Hz
		001	50 Hz
		010	60 Hz
		011	100 Hz
		100	500 Hz
		101	1000 Hz
		110	2000 Hz
		111	3750 Hz
5 - 7	Reserved	0	

Relationship between gain and the measurement range

Gain	Measurement range	Measurement range x bridge voltage
1	±125 mV/V	±0.553 V
2	±62.500 mV/V	±0.278 V
3	±31.250 mV/V	±0.136 V
4	±15.625 mV/V	±0.069 V

7.4.9.2 X67UM4389

Register	Name	Bytes	Module			
			X67UM4389 X67UM4389-C10		X67UM4389-C01 X67UM4389-C11	
Input:						
0	Digital inputs 1 - 8	1	Byte		Byte	
1	Digital inputs 9 - 12 and digital outputs 1 - 4	1	Byte		Byte	
30	Status of the outputs[1)]	1				
Output:						
2	**HI:** 0 **LO:** Digital outputs 1 - 4	1 / 2		Word		Byte
4	Analog outputs 1	1		Word		
6	Analog outputs 2	1		Word		
8	Analog outputs 3	1		Word		
10	Analog outputs 4	1		Word		
Data bytes in DP frame			2 in	10 out	2 in	1 out

1) Diagnostics information is automatically sent to the PROFIBUS DP master.

Digital inputs 1 - 8

This register is used to indicate the input state of digital inputs 1 to 8. As a result, the input with the lowest channel number is located in the LSB; the bits of the inputs that are not present are 0.

Bit	Name	Value	Information
0	Channel 1	0 or 1	Input state - Digital input 1
...		...	
7	Channel 8	0 or 1	Input state - Digital input 8

Digital inputs 9 - 12 and digital outputs 1 - 4

This register is used to indicate the input state of the digital inputs 9 to 12 and the status of the digital outputs 1 to 4.

Bit	Name	Value	Information
0	Channel 9	0 or 1	Input state - Digital input 9
...		...	
3	Channel 12	0 or 1	Input state - Digital input 12
4	Status - Digital output 1	0	No error
		1	Current output value is not identical to the set value
...		...	
7	Status - Digital output 4	0	No error
		1	Current output value is not identical to the set value

Status of the outputs

This register is used to indicate the status of the digital and analog outputs.

Bit	Name	Value	Information
0	Digital output 1	0	No error
		1	Current output value is not identical to the set value
...		...	
3	Digital output 4	0	No error
		1	Current output value is not identical to the set value
4	Analog output 1	0	No error
		1	Set value on output 1 is <0
...		...	
7	Analog output 4	0	No error
		1	Set value on output 4 is <0

Digital outputs

This register is used to indicate the output status of the digital outputs. As a result, the output with the lowest channel number is located in the LSB in each case; the bits of the channels configured as input are ignored when set.

Bit	Name	Value	Information
0	Channel 1	0	Digital output reset
		1	Digital output set
...		...	
3	Channel 4	0	Digital output reset
		1	Digital output set
4 - 7	Reserved	-	

Analog outputs

These registers provide the analog output values. Only positive values can be set here. When attempting to output a negative value, the value 0 is output and the corresponding bit is set in the Status of the outputs register.

Values	Information
-32,768 to 32,767	Only positive values possible

7.4.9.3 X67UM4389-C01

Register	Name	Bytes	Module	
			X67UM4389-D01 X67UM4389-D11	
Input:				
0	Digital inputs 1 - 8	1	Byte	
1	Digital inputs 9 - 12 and digital outputs 1 - 4	1	Byte	
30	Status of the outputs[1)]	1		
Output:				
2	Digital outputs 1 - 4	1		Byte
Data bytes in DP frame			2 in	1 out

1) Diagnostics information is automatically sent to the PROFIBUS DP master.

Digital inputs 1 - 8

This register is used to indicate the input state of digital inputs 1 to 8. As a result, the input with the lowest channel number is located in the LSB; the bits of the inputs that are not present are 0.

Bit	Name	Value	Information
0	Channel 1	0 or 1	Input state - Digital input 1
...		...	
7	Channel 8	0 or 1	Input state - Digital input 8

Digital inputs 9 - 12 and digital outputs 1 - 4

This register contains the input state of digital inputs 9 to 12 and the state of digital outputs 1 to 4.

Bit	Name	Value	Information
0	Channel 9	0 or 1	Input state - Digital input 9
...		...	
3	Channel 12	0 or 1	Input state - Digital input 12
4	Status - Digital output 1	0	No error
		1	Current output value is not identical to the set value
...		...	
7	Status - Digital output 4	0	No error
		1	Current output value is not identical to the set value

Status of the outputs

This register contains the state of the digital and analog outputs.

Bit	Name	Value	Information
0	Digital output 1	0	No error
		1	Current output value is not identical to the set value
...		...	
3	Digital output 4	0	No error
		1	Current output value is not identical to the set value
4 - 7	Reserved	-	

Digital outputs 1 - 4

This register contains the output state of the digital outputs. As a result, the output with the lowest channel number is located in the LSB in each case; the bits of the channels configured as input are ignored when set.

Bit	Name	Value	Information
0	Channel 1	0	Digital output reset
		1	Digital output set
...		...	
3	Channel 4	0	Digital output reset
		1	Digital output set
4 - 7	Reserved	-	

7.4.10 Temperature modules

7.4.10.1 X67AT13xx

Register	Name	Bytes	Module							
			X67AT1311 X67AT1311-C01 X67AT1322-C01		X67AT1322-C02		X67AT1322-C03		X67AT1322-C04	
Input:										
0	Temperature value input 1	2	Word		Word		Word		Word	
2	Temperature value input 2	2	Word		Word		Word		Word	
4	Temperature value input 3	2	Word		Word		Word		Word	
6	Temperature value input 4	2	Word		Word		Word		Word	
30	Input status	2			Word				Word	
Output:										
16	**HI: 0** **LO:** Filter parameter	2		1)		1)		Word		Word
18	Configure sensor type	2		1)		1)		Word		Word
Data bytes in DP frame			8 in	0 out	10 in	0 out	8 in	4 out	10 in	4 out

1) The register is transferred acyclically.

Temperature value input

The module stores converted analog values in these registers. In order for the user to always be supplied with a defined output value, the output value is predefined in various conditions:

- Up to the first conversion, 0x8000 is output.
- After switching the operating mode until the first conversion:
  - From "Resistance measurement" to "Sensor type PTxx": 0x8000
  - From "Sensor type PTxx" to "Resistance measurement": 0xFFFF
- If the input is not switched on, 0x8000 is output.

Conversion cycle

All pending signals from enabled inputs are converted to digital values in every conversion cycle.

Unnecessary inputs can be disabled to reduce the I/O update time. Inputs can also be disabled temporarily if they are not needed for a certain amount of time.

The conversion time needed for an individual input is calculated using the following formula:

$$3 \times \frac{1}{filter\ frequency} + 15\ ms$$

The time saved per disabled input depends on the selected filter:

Filter frequency	Filter time	Time saved per input	Digital converter resolution
50 Hz	20 ms	75 ms	16-bit
60 Hz	16.67 ms	65 ms	16-bit
250 Hz	4 ms	27 ms	13-bit
500 Hz	2 ms	21 ms	10-bit

Example

	Example 1	Example 2
Switched on inputs	1 to 4	1 and 3
Conversion time	300 ms	150 ms

Input status

This register returns acyclic diagnostics messages such as open line or measurement range exceeded. If an error occurs a diagnostics message will be sent. The information in models **-C02** and **-C04** is transferred with the cyclic data.

Bit	Name	Value	Information
0 - 1	Channel 1	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
...		...	
6 - 7	Channel 4	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
8 - 15	Number of previous conversion cycles		

In addition to the status info, the error type also sets the respective analog value as follows:

Error status	Temperature measurement Digital value for error	Resistance measurement Digital value for error
Open line	+32767 (0x7FFF)	65535 (0xFFFF)
Upper limit value exceeded	+32767 (0x7FFF)	65535 (0xFFFF)
Lower limit value exceeded	-32767 (0x8001)	0 (0x0000)
Invalid value	-32768 (0x8000)	65535 (0xFFFF)

Filter parameter

This register makes it possible to set the filter frequency. This affects all inputs globally. In models **-C03** and **-C04**, this parameter is transferred in the cyclic data as a word; only the low byte is used for the configuration.

Value (decimal)	Filter frequency
0	50 Hz
1	60 Hz
2	250 Hz
3	500 Hz

Configure sensor type

This register is used to configure the sensor type and respectively the setting of the raw value measurements (without linearization and terminal temperature compensation) and to disable individual inputs in order to keep the conversion time down. This parameter simultaneously applies to all channels. In models **-C03** and **-C04**, this parameter is transferred as one word in the cyclic data.

Bit	Function	Value	Information
0 - 3	Input 1	0000	Sensor type KTY10
		0001	Sensor type KTY84
		0010	Sensor type PT100
		0011	Sensor type PT1000
		0100	Reserved
		0101	Resistance measurement 0.1 to 4500
		0110	Resistance measurement 0.05 to 2250
		0111	Input disabled
4 - 7	Input 2	x	Values same as input 1
8 - 11	Input 3	x	Values same as input 1
12 - 15	Input 4	x	Values same as input 1

7.4.10.2 X67AT1402

Register	Description	Bytes	Module							
			X67AT1402-C01		X67AT1402-C02		X67AT1402-C03		X67AT1402-C04	
Input:										
0	Temperature value input 1	2	Word		Word		Word		Word	
2	Temperature value input 2	2	Word		Word		Word		Word	
4	Temperature value input 3	2	Word		Word		Word		Word	
6	Temperature value input 4	2	Word		Word		Word		Word	
30	Input status	2			Word				Word	
Output:										
16	Filter parameter	1		1)		1)		Byte		Byte
18	Configure sensor type	1		1)		1)		Byte		Byte
Data bytes in DP frame			8 in	0 out	10 in	0 out	8 in	2 out	10 in	2 out

1) The register is transferred acyclically.

Temperature value input

The module stores converted analog values in these registers. In order for the user to always be supplied with a defined output value, the output value is predefined in various conditions:

	Temperature measurement	Resistance measurement
Predefined output value – Until the first conversion – After switching over the measurement range until the first conversion – If the input is disabled	0x8000	0xFFFF
– No temperature sensor is used with sensor types J, K or S	0x7FFF	0x7FFF

Raw value measurement

Raw value measurement functions with and without terminal temperature measurement. If another sensor type is used as J, K and S, then the terminal temperature must be measured on at least one input. Based on this value, the user must then implement terminal temperature compensation.

Conversion cycle

The timing for acquiring measurement values is determined by the converter hardware. All enabled inputs are converted during each conversion cycle. A terminal temperature measurement also takes place.

Unnecessary inputs can be switched off, thereby reducing the refresh time. Inputs can also be only switched off temporarily. The measurement of the terminal temperature cannot be switched off.

The amount of time saved per channel depends on the filter time:

Filter	Filter time	Amount of time saved per input	Digital converter resolution
50 Hz	20 ms	75 ms	16-bit
60 Hz	16.67 ms	65 ms	16-bit
250 Hz	4 ms	27 ms	13-bit
500 Hz	2 ms	21 ms	10-bit

Examples

Inputs are filtered using a 50 Hz filter.

	Example 1	Example 2
Switched on inputs	1 - 4	1, 3
Conversion time for inputs	248 ms	124 ms
Conversion time for terminal temperature	62 ms	62 ms
Conversion time total	310 ms	186 ms

Input status

This register returns acyclic diagnostics messages such as open line or measurement range exceeded. If an error occurs a diagnostics message will be sent. This diagnostics function can be enabled or disabled using the parameter "Channel Diagnose x". In the models **-C02** and **-C04**, this information is transferred with the cyclic data.

Bit	Name	Value	Information
0 - 1	Channel 1	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
...		...	
6 - 7	Channel 4	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
8 - 15	Number of previous conversion cycles		

In addition to the status info, the error type also sets the respective analog value as follows:

Error status	Digital value for error
Open line	+32767 (0x7FFF)
Upper limit value exceeded	+32767 (0x7FFF)
Lower limit value exceeded	-32767 (0x8001)
Invalid value	-32768 (0x8000)

Filter parameter

This register makes it possible to set the filter frequency. This affects all inputs globally. In models **-C03** and **-C04**, this parameter is transferred in the cyclic data as a word; only the low byte is used for the configuration.

Value (decimal)	Filter frequency
0	50 Hz
1	60 Hz
2	250 Hz
3	500 Hz

Configure sensor type

This register is used to configure the sensor type and respectively the setting of the raw value measurements (without linearization and terminal temperature compensation) and to disable individual inputs in order to keep the conversion time down. This parameter simultaneously applies to all channels. In models **-C03** and **-C04**, this parameter is transferred to the cyclic data as a byte.

Bit	Name	Value	Information
0 - 2	Sensor type	000	No sensor used
		001	Sensor type J
		010	Sensor type K
		011	Sensor type S
		100 to 101	No sensor used
		110	Raw value measurement: Resolution 1 µV for a measurement range of ±32.767 mV
		111	Raw value measurement: Resolution 2 µV for a measurement range of ±65.534 mV
3	Reserved	0	
4	Input 1	0	Input 1 switched on
		1	Input 1 switched off
...		...	
7	Input 4	0	Input 4 switched on
		1	Input 4 switched off

7.4.11 Counter modules

7.4.11.1 X67DC1198

Register	Name	Bytes	Module			
			X67DC1198-C01		X67DC1198-C11	
Input:						
3104	ABR counter (connection 1, channel 9 - 11)	2	Word		Word	
40	**HI:** Status of encoder supply	2	Word		Word	
3142	**LO:** ABR status of the homing procedure					
7440	SSI position (connection 3, channel 13 = data, channel 15 = clock)	4	Long		Long	
2080	AB counter 1 (connection 1, channel 1 - 2)	2	Word		Word	
2336	AB counter 2 (connection 2, channel 3 - 4)	2	Word		Word	
2592	AB counter (connection 3, channel 5 - 6)	2	Word		Word	
2852	Event counter (connection 4, channel 8)	2	Word		Word	
4422	Period measurement (channel 9)	2			Word	
Output:						
6162	PWM output (connection 4, channel 7)	2		Word		Word
3140	**HI:** 0 **LO:** ABR referencing mode	2		Word		Word
3088	ABR homing position	2		1)		1)
3136	ABR reference pulse	1		1)		1)
7432	SSI configuration	2		1)		1)
6160	PWM cycle time	2		1)		1)
2826	Counting direction	1		1)		1)
Data bytes in DP frame			16 in	4 out	18 in	4 out

1) The register is transferred acyclically.

ABR counter

These registers indicate the counter value of the encoder as a 16-bit value on module connection 1 (channel 9 to 11).

Value	Information
-32,768 to 32,767	Counter value

Status of encoder supply

This register indicates the status of the integrated encoder supply. A faulty encoder power supply is displayed as a warning.

Bit	Name	Value	Information
0	Internal supply	0	5 VDC internal supply voltage OK
		1	5 VDC internal supply voltage faulty
1	Encoder supply	0	24 VDC encoder power supply OK
		1	24 VDC encoder power supply faulty
2 - 7	Reserved	-	

ABR status of the homing procedure

This register contains the homing state of the ABR encoder.

Bit	Description	Value	Information
0 - 1	Reserved	0	
2	Bit is always 1 after the first reference pulse.	0	No reference pulses have occurred since the start of referencing.
		1	The first reference pulse has occurred.
3	State change when referencing is complete	0 or 1	State change when referencing is complete
4	Bit is always 1 after the first reference pulse.	0	No reference pulses have occurred since the start of referencing.
		1	The first reference pulse has occurred.
5 - 7	Continuous counter	xxx	Increased with each reference pulse

Examples of possible values

0b00000000	= 0x00	Referencing OFF or homing procedure already active
0b00111100	= 0x3C	First reference complete, reference value applied in the ABR counter register.
0bxxx11100	= 0xxB	Bits 5 to 7 are changed with each reference pulse
0bxxx1x100	= 0xxx	Bits changed continuously with the setting continuous referencing. With every reference pulse, the reference value is applied to the ABR counter register.

SSI position

The last transferred SSI position can be read out from this register. The SSI encoder value is displayed as a 32-bit position value. This position value is generated synchronously with the X2X cycle.

Value	Information
0 to 4,294,967,295	Last SSI position transferred

AB counter

These registers are used to indicate the counter value for the encoder on the module connections for channel 1 to 6.

Value	Information
-32,768 to 32,767	Counter value

Event counter

This register indicates the counter value of the event counter as a 16-bit value on module connection 4 (channel 8).

Value	Information
-32,768 to 32,767	Encoder position or counter value

Period measurement

The GSD model **X67DC1198-C11** activates a special function model of the I/O module thereby making it possible to carry out period measurement.

This register makes it possible to determine the period time of the encoder revolution on the A-track of the ABR incremental encoder. The time between 2 falling edges is represented as 16 bit value.

Value
0 to 65,535

PWM output

In this register, a configuration is made for the percentage of the PWM cycle (in 1/10 % steps) that the PWM output is logical 1, i.e. ON.

Value	Information
0	PWM output always off
2 to 999	Turn on time in 1/10% steps
1000	PWM output always on

ABR referencing mode

The bits in this register are used to configure the reaction to the configured reference pulse.

Bit	Description	Value	Information
0 - 1	Sets the referencing mode	00	Referencing OFF
		01	Single shot referencing
		10	Reserved
		11	Continuous referencing
2 - 5	Reserved	-	
6 - 7	Reserved	11	Must always be 11!

This results in the following values:

0b00000000	= 0x00	Referencing OFF
0b11000001	= 0xC1	Single shot referencing →When starting over after the referencing process is complete, the value 0x00 must be written to start again. Wait until the ABR status of the homing procedure register also takes on the value 0x00. Only then is value 0xC1 permitted to be written again.
0b11000011	= 0xC3	Continuous referencing →Referencing takes place automatically with every reference pulse

ABR homing position

These registers can be used to define an offset value for referencing. (High byte = counter value homing position / 256 (without remainder), Low byte = remainder * 256)

Values
-32,768 to 32,767

ABR reference pulse

This register configures whether a rising or falling edge is used to trigger referencing.

Value	Information
4106	Falling edge
4122	Rising edge

SSI configuration

This configuration register is used to set the coding, the clock rate and the number of bits.
Default = 0.

Bit	Name	Value	Information
0 - 5	SSI value valid bits	x	
6 - 7	Clock rate	11	125 kHz
8 - 13	SSI number of bits	x	Number of bits including leading zeros
14	Reserved	0	
15	Keying	0	Binary coding
		1	Gray coding

PWM cycle time

The length of the PWM cycle is configured using this register. The base is a 48 MHz clock, which can be changed (divided) using the setting in this register. One PWM cycle consists of 1,000 of the resulting clocks after they have been divided. The period duration of the PWM cycle is calculated as follows:

$$PWM_cycle = 1000 \frac{prescale}{48000000} [s]$$

Value	Information
2 to 65,535	Prescaler for PWM cycle. The PWM function of the module is specified for a period length greater than 500 µs.

Example

Value	Period duration	Frequency
2	41.6 µs	24 kHz
24,000	500 ms	2 Hz
48,000	1 s	1 Hz
65,535	1.36 s	0.73 Hz

Counting direction

The counting direction for the counter function can be configured in these registers.

Value	Information
0	Upwards
1	Downwards

7.5 Additional X2X I/O modules

7.5.1 Keypad modules

7.5.1.1 4XP0000.00-K12 / K39 / K47

Register	Name	Bytes	Module					
			Extension 40 keys		Extension 27 keys		Extension 24 keys	
			4XP0000.00-K12		4XP0000.00-K47		4XP0000.00-K39	
Input:								
0	Key input	2	Word		Word		Word	
2	Key input	2	Word		Word		Word	
4	Key input	2	Word		Word			
6	Key input	2	Word					
8	Key input	2	Word					
Output:								
0	LED output	2		Word		Word		Word
2	LED output	2		Word		Word		Word
4	LED output	2		Word		Word		Word
6	LED output	2		Word		Word		Word
8	LED output	2		Word		Word		Word
10	LED output	2		Word		Word		
Data bytes in DP frame			10 in	12 out	6 in	12 out	4 in	10 out

7.5.1.2 4XP0000.00-K19 / K20 / K30 / K40 /K95

Register	Name	Bytes	Module					
			Extension 2 keys 4 XP 0000.00-K19		Extension 4 keys 4 XP 0000.00-K20 4 XP 0000.00-K40		Extension 4 keys 4 XP 0000.00-K30 4 XP 0000.00-K95	
Input:								
0	Key input	1	Byte				Byte	
4	Key input	1			Byte			
Output:								
0	LED output	1 / 2		Byte		Word		Word
Data bytes in DP frame			1 in	1 out	1 in	2 out	1 in	2 out

7.5.1.3 4XP0000.00-K21 / K22 / K41 / K46

Register	Name	Bytes	Module					
			Extension 6 keys 4XP0000.00-K21 4XP0000.00-K41		Extension 6 keys 4XP0000.00-K22		Extension 21 keys 4XP0000.00-K46	
Input:								
0	Key input	2					Word	
2	Key input	2					Word	
4	Key input	1	Byte		Byte			
Output:								
0	LED output	2		Word		Word		Word
2	LED output	2		Word				Word
4	LED output	2						Word
6	LED output	2						Word
8	LED output	2						Word
Data bytes in DP frame			1 in	4 out	1 in	2 out	4 in	10 out

7.5.1.4 4XP0000.00-K62

Register	Name	Bytes	Module 4XP0000.00-K62	
Input:				
0	Keys 1 - 12	2	Word	
2	Keys 17 - 20	2	Word	
4	Digital inputs 1 - 3	2	Word	
Output:				
0	LED output 1 - 8	2		Word
2	LED output 9 - 16	2		Word
4	LED output 17 - 24	2		Word
6	LED output 25 - 32	2		Word
8	LED output 33 - 40	2		Word
10	7-segment display	2		Word
12	7-segment display	2		Word
14	7-segment display	2		Word
	Data bytes in DP frame		6 in	16 out

7.5.1.5 4XP0000.00-K64 / K74 / K75

Register	Name	Bytes	Module Extension 6 keys 4XP0000.00-K64 4XP0000.00-K74 4XP0000.00-K75	
Input:				
0	Key input	1	Byte	
Output:				
0	LED output	2		Word
2	LED output	1		Byte
	Data bytes in DP frame		1 in	3 out

7.5.1.6 4XP0000.00-K76 / K94 / KA4

Register	Name	Bytes	Module 4XP0000.00-K76 4XP0000.00-K94 4XP0000.00-KA4	
Input:				
0	Key input	1	Byte	
Output:				
0	**MSB**: LED3 - LED4	2		Word
	LSB: LED1 - LED2			
2	**MSB**: LED5 - LED6	1		Byte
	Data bytes in DP frame		1 in	3 out

7.5.1.7 4XP0000.00-K85

Register	Name	Bytes	Module 4XP0000.00-K85	
Input:				
0	**MSB**: Keys 9 - 16	2	Word	
	LSB: Keys 1 - 8			
Output:				
0	**MSB**: LED 3 - LED 4	2		Word
	LSB: LED 1 - LED 2			
4	**MSB**: LED 7 - LED 8	2		Word
	LSB: LED 5 - LED 6			
8	**MSB**: LED 11 - LED 12	2		Word
	LSB: LED 9 - LED 10			
12	**MSB**: LED 15 - LED 16	2		Word
	LSB: LED 13 - LED 14			
	Data bytes in DP frame		2 in	8 out

7.5.1.8 4XP0101.00-00x

Register	Description	Bytes	Module 4XP0101.00-00x	
Input:				
0	Key input	1	Byte	
Output:				
0	LED output 1 - 4	2		Word
2	LED output 5 - 8	2		Word
Data bytes in DP frame			1 in	4 out

7.5.2 Keypad extension for APC

7.5.2.1 5ACCKP01.185B-C01 / .240C-C01

Register	Name	Bytes	Module 5ACCKP01.185B-C01 5ACCKP01.240C-C01	
Input:				
0	Key input	1	Byte	
Output:				
0	LED output	2		Word
Data bytes in DP frame			1 in	2 out

7.5.2.2 5AC800.EXT3

Register	Name	Bytes	Module			
			Extension 8 keys		Extension 12 keys	
			5AC800.EXT 3-00/-01 5AC800.EXT 3-10/-11		5AC800.EXT 3-02/-03 5AC800.EXT 3-12/-13	
Input:						
33	Key input	1	Byte		Byte	
35	Key input	1	Byte			
61	Key input	1	Byte		Byte	
63	Key input	1	Byte		Byte	
Output:						
1	LED output	1		Byte		Byte
5	LED output	1		Byte		Byte
9	LED output	1		Byte		Byte
13	LED output	1		Byte		Byte
17	LED output	1		Byte		
21	LED output	1		Byte		
25	LED output	1		Byte		
29	LED output	1		Byte		Byte
31	LED output	1		Byte		Byte
Data bytes in DP frame			4 in	9 out	3 in	6 out

7.5.2.3 5AC800.EXT3-K03

Register	Name	Bytes	Module Extension 18 keys 5AC800.EXT 3-K03	
Input:				
57	Key input	1	Byte	
59	Key input	1	Byte	
61	Key input	1	Byte	
63	Key input	1	Byte	
Output:				
1	LED output	1		Byte
3	LED output	1		Byte
5	LED output	1		Byte
7	LED output	1		Byte
31	LED output	1		Byte
Data bytes in DP frame			4 in	5 out

7.5.2.4 5AC800.EXT3-K05

Register	Name	Bytes	Module Extension 18 keys 5AC800.EXT 3-K05	
Input:				
33	Key input	1	Byte	
35	Key input	1	Byte	
37	Key input	1	Byte	
Output:				
1	LED output	1		Byte
3	LED output	1		Byte
5	LED output	1		Byte
7	LED output	1		Byte
9	LED output	1		Byte
Data bytes in DP frame			3 in	5 out

7.5.3 Keypad extension for panels

7.5.3.1 5AP933.156B-K10

Register	Description	Bytes	Module 5AP933.156B-K10	
Input:				
0	Key input	1	Byte	
6	Encoder	2	Word	
Output:				
0	LED output	1		Byte
18	LED output	1		Byte
Data bytes in DP frame			3 in	2 out

7.5.3.2 5AP93D.156B-K02

Register	Name	Bytes	Module 5AP93D.156B-K02	
Input:				
0	Key input	1	Word	
Output:				
0	LED output	2		Word
2	LED output	2		Word
4	LED output	2		Word
Data bytes in DP frame			2 in	6 out

7.5.3.3 5AP980.1505-B10

Register	Name	Bytes	Module 5AP980.1505-B10	
Input:				
0	**MSB:** Keys 9 to 14 and 22 **LSB:** Keys 1 to 8	2	Word	
2	**MSB:** Nothing **LSB:** Keys 15 to 21	2	Word	
Output:				
0	**MSB:** LED 9 to 16 **LSB:** LED 1 to 8	2		Word
2	**MSB:** LED 25 to 32 **LSB:** LED 17 to 24	2		Word
4	**MSB:** Nothing **LSB:** LED 33 to 40	2		Word
Data bytes in DP frame			4 in	6 out

7.5.3.4 5PC725.1505-K01X2X

Register	Name	Bytes	Module Extension 6 keys 5PC725.1505-K01X2X	
Input:				
0	Key input	2	Word	
Output:				
0	LED output	2		Word
2	LED output	2		Word
Data bytes in DP frame			2 in	4 out

7.5.3.5 5PP320.1043.K03

Register	Name	Bytes	Module 5PP320.1043.K03	
Input:				
0	Key input	1	Byte	
Output:				
0	LED output	1		Byte
Data bytes in DP frame			1 in	1 out

7.5.4 Valve connections

7.5.4.1 0AC190.1-NOR

Register	Name	Bytes	Module					
			0AC190.1-NOR-C01		0AC190.1-NOR-C02		0AC190.1-NOR-C03*	
Input:								
10	Valves connected (block 1 + 2)	1					Byte	
11	Valves connected (block 3 + 4)	1					Byte	
12	Valves connected (block 5 + 6)	1					Byte	
13	Valves connected (block 7 + 8)	1					Byte	
14	Valves connected (block 9 + 10)	1					Byte	
15	Status of digital outputs (block 1 + 2)	1			Byte		Byte	
16	Status of digital outputs (block 3 + 4)	1			Byte		Byte	
17	Status of digital outputs (block 5 + 6)	1			Byte		Byte	
18	Status of digital outputs (block 7 + 8)	1			Byte		Byte	
19	Status of digital outputs (block 9 + 10)	1			Byte		Byte	
30	Overall status	1					Byte	
Output:								
0	Digital outputs (block 1 + 2)	1		Byte		Byte		Byte
1	Digital outputs (block 3 + 4)	1		Byte		Byte		Byte
2	Digital outputs (block 5 + 6)	1		Byte		Byte		Byte
3	Digital outputs (block 7 + 8)	1		Byte		Byte		Byte
4	Digital outputs (block 9 + 10)	1		Byte		Byte		Byte
Data bytes in DP frame			0 in	5 out	5 in	5 out	11 in	5 out

Module names with '*': Support with firmware version ≥ V1.43

Valves connected

This register indicates whether the valves of the affected block are connected.

Status of digital outputs

This register indicates the state of the digital outputs for the affected block.

Overall status

Bit	Description
0	Valve voltage overflow state
1	Valve voltage underflow state
2	Vcc underflow state
3	Hardware monitoring state
4	Valve total overflow state
5	Valves not connected state - Composite error
6	Reserved
7	I/O bus error state

Digital outputs

This register indicates the output state of the digital outputs for the affected block.

7.5.4.2 7XV1xx.50-xx

Register	Name	Bytes	Module					
			7XV108.50-xx		7XV116.50-xx		7XV124.50-xx	
Input:								
0	Status of the outputs	1	Byte		Byte		Byte	
Output:								
0	Digital outputs 1 - 8	1		Byte		Byte		Byte
1	Digital outputs 9 - 16	1				Byte		Byte
2	Digital outputs 17 - 24	1						Byte
	Data bytes in DP frame		1 in	1 out	1 in	2 out	1 in	3 out

Status of the outputs

Tis register signals overload on the outputs or problems with the module supply.

Bit	Name	Value	Description
0	24 VDC supply monitor	0	Outside of the permitted range
		1	OK
1	Monitoring the outputs	0	Overload on one or more outputs
		1	OK
2	Reserved	-	Always 1
3 - 7	Reserved	-	Always 0

Digital outputs

This register is used to indicate the output status of the digital outputs.

7.5.5 Compact I/O

7.5.5.1 7XX408.50-1

Register	Name	Bytes	Module							
			Digital I/O				Digital I/O + counters + PWM			
			7XX408.50-1-C01		7XX408.50-1-C02		7XX408.50-1-C12		7XX408.50-1-C14	
Input:										
0	Digital inputs 1 - 8	1	Byte		Byte		Byte		Byte	
1	Digital inputs 9 - 16	1	Byte		Byte		Byte		Byte	
2	Status of digital outputs 1 - 8	1	Byte		Byte		Byte		Byte	
3	Status of digital outputs 9 - 16	1	Byte		Byte		Byte		Byte	
4	Counter (32-bit)	4					Long		Long	
8	Counter (16-bit)	2					Word		Word	
30	Module status	2			Word		Word		Word	
Output:										
2	Digital outputs 1 - 8	1		Byte		Byte		Byte		Byte
3	Digital outputs 9 - 16	1		Byte		Byte		Byte		Byte
20	PWM period	2						Word		Word
22	Pulse width 15	2						Word		Word
24	Pulse width 16	2						Word		Word
26	Module configuration	2						1)		Word
Data bytes in DP frame			4 in	2 out	6 in	2 out	12 in	8 out	12 in	10 out

1) The register can be modified in the parameter dialog box for the I/O module and is transferred acyclically.

Digital inputs

This register is used to indicate the status of the digital inputs.

Bit	Name	Value	Information
0	Channel 1 (or 9)	0 or 1	Input state - Digital input 1 or 9
...		...	
x	Channel 1 (or 9) + x	0 or 1	Input state - Digital input 1 or 9 + x

Status of digital outputs

This register is used to indicate the status of the digital outputs.

Bit	Name	Value	Information
0	Channel 1 (or 9)	0	Digital output reset
		1	Digital output set
...		...	
x	Channel 1 (or 9) + x	0	Digital output reset
		1	Digital output set

Counter

The configuration register must be set in order to set the correct counter modes. Counter 1 and counter 2 registers have different meanings for different modes.

Incremental encoder operation

If the reference input (digital input 3) in the configuration register is enabled, then the module is a 16-bit ABR counter whose actual value is located in counter 1 (only LW) and the stored R-value in counter2 (functions as latch).

If the reference input is not active, then it is a 32-bit AB incremental encoder counter input that should be read with counter 1 (LW and HW).

Assignment of the digital inputs 1 to 3:

- A = Input 1
- B = Input 2
- R = Input 3

Event counter operation

If the counters are initialized as event counters in the configuration register, we get a 32-bit counter (counter 1 LW +HW) and a 16-bit counter (counter 2):

- Input 1 = Counter 1
- Input 2 = Counter 2

Period measurement

The measurement can be begin at the decreasing or increasing edge depending on the configuration register. The R mode bit must be 0. Measurement always occurs up to the next identical edge. The pauses between 2 period measurements must last for at least 2 periods of the counter frequency. The counter frequency can be set to one of 2 levels (4 MHz or 31.25 kHz) or with an external frequency. The external frequency must be <50 kHz, however. The measured counter state is a 16-bit value and is displayed in counter 1 (only LW). The value in the temporary register is only updated at the end of the active measurement.

The frequency of the signal to be measured can be a maximum of 50 kHz.

Assignment of the digital inputs:

- Input 1 = measurement input
- Input 2 = external counter frequency

If an overflow of the continuous counter occurs during the period measurement (e.g. due to an incorrect counter frequency), this can be detected by setting bit 9 in the configuration register. The maximum value of the counter is limited to 0x7FFF, however. The error bit in the status register is acknowledged by resetting bit 9 of the configuration register.

Gate measurement

The measurement can be begin at the decreasing or increasing edge depending on the configuration register. The R mode bit must be 0. Measurement always occurs up to the next edge. The pauses between 2 gate measurements must last for at least 2 periods of the counter frequency. The counter frequency can be set to one of 2 levels (4 MHz or 31.25 kHz) or with an external frequency. The external frequency must however be < 50 kHz. The measured counter state is a 16-bit value and is displayed in counter 1 (only LW). The value in the temporary register is only updated at the end of the active measurement.

The frequency of the signal to be measured can be a maximum of 25 kHz.

Assignment of the digital inputs:

- Input 1 = measurement input
- Input 2 = external counter frequency

If an overflow of the continuous counter occurs during gate measurement (e.g. due to an incorrect counter frequency), this can be detected by setting bit 9 in the configuration word. The maximum value of the counter is limited to 0x7FFF, however. The error bit in the status word is acknowledged by resetting bit 9 of the configuration word.

Module status

Bit	Description	Value	Information
0 - 8	Reserved	0	(must be 0)
9	R mode	0	Period or gate measurement within the counter range 0 to 0x7FFF (only valid if bit 9 is set in the configuration register)
		1	Counter overflow during period or gate measurement, acknowledged by resetting bit 9 of the configuration word
10	Reserved	0	(must be 0)
11	Monitoring the module supply voltage	0	Module power supply OK (within the limits 18 V to 30 V)
		1	Error (module power supply outside the limits)
12	Input voltage monitoring	0	DC OK OK
		1	DC OK error
13	Summation current monitoring of digital outputs 13 and 14:	0	<4 A
		1	>4 A
14	Summation current monitoring of digital outputs 15 and 16:	0	<4 A
		1	>4 A
15	Monitoring of the output supply	0	24 VDC OK
		1	24 VDC error

Digital outputs

This register is used to indicate the output status of the digital outputs.

As a result, the output with the lowest channel number is located in the LSB; the bits of the outputs that are not present are ignored by the module.

Bit	Name	Value	Information
0	Channel 1 (or 9)	0	Digital output reset
		1	Digital output set
...		...	
x	Channel 1 (or 9) + x	0	Digital output reset
		1	Digital output set

PWM period

The period can be set between 1 and 1000 ms. The decimal value 1000 corresponds to a period of 1 sec.

Pulse width

The pulse width (pulse width 15 and pulse width 16) can be set in 0.1% steps between 0% and 100%. The decimal value 1000 corresponds to a pulse width of 100%.

Module configuration

Bit	Description	Value	Information
0	Reserved	0	(must be 0)
1	R mode	0	R disabled (in AB(R) mode, see bit 4 and 5)
		1	R enabled (in AB(R) mode)
2	Type of measurement	0	Period measurement
		1	Gate measurement
3	Measurement starts	0	Measurement starts at increasing edge
		1	Measurement starts at falling edge
4 - 5	Mode	00	No counter operation
		01	AB(R) counter
		10	Event counter
		11	Period or gate measurement
6 - 7	Counter frequency	00	4 MHz
		01	External (input 3)
		10	32.25 kHz
		11	Not permitted
8	Reserved	0	(must be 0)
9	Overflow recognition	0	Disabled (reset counter overflow bit in configuration register)
		1	Enabled (value of the counter is limited to 0x7FFF when overflow)
10 - 13	Reserved	0	(must be 0)
14	PWM function	0	Off
		1	On
15	Time/Counter	0	Reset time/counter
		1	Time/Counter enabled (set bit only after completion of counter configuration)

7.5.5.2 7XX436.50-1

Register	Name	Bytes	Module							
			Digital I/O + analog I/O				Digital I/O + analog I/O + counters + PWM			
			7XX436.50-1-C01		7XX436.50-1-C02		7XX436.50-1-C12		7XX436.50-1-C14	
Input:										
0	Digital inputs 1 - 8	2	Word		Word		Word		Word	
8	Status of digital outputs	2	Word		Word		Word		Word	
24	Analog input (multi) 1	2	Word		Word		Word		Word	
26	Analog input (multi) 2	2	Word		Word		Word		Word	
28	Analog input (single) 3	2	Word		Word		Word		Word	
30	Analog input (single) 4	2	Word		Word		Word		Word	
16	Counter (32-bit)	4					Long		Long	
20	Counter (16-bit)	2					Word		Word	
36	Trigger value	2					Word		Word	
38	Trigger timestamp	2					Word		Word	
32	Module status	2			Word		Word		Word	
Output:										
0	Digital outputs 1 - 8	2		Word		Word		Word		Word
24	Analog output 1	2		Word		Word		Word		Word
26	Analog output 2	2		Word		Word		Word		Word
28	Analog output 3	2		Word		Word		Word		Word
30	Analog output 4	2		Word		Word		Word		Word
16	PWM period	2						Word		Word
18	Pulse width 1	2						Word		Word
20	Pulse width 2	2						Word		Word
32	Module configuration	2						[1]		Word
36	Trigger level	2						Word		Word
38	Comparator output	2						Word		Word
Data bytes in DP frame			12 in	10 out	14 in	10 out	24 in	20 out	24 in	22 out

1) The register can be modified in the parameter dialog box for the I/O module and is transferred acyclically.

Digital inputs

This register is used to indicate the status of the digital inputs.

Bit	Name	Value	Information
0	Channel 1	0 or 1	Input state - Digital input 1
...		...	
7	Channel 8	0 or 1	Input state - Digital input 8

Status of digital outputs

This register is used to indicate the status of the digital outputs.

Bit	Name	Value	Information
0	Channel 1	0	Digital output reset
		1	Digital output set
...		...	
7	Channel 8	0	Digital output reset
		1	Digital output set

Analog input (multi)

The analog input value is mapped in this register.

The following values are measured based on the configuration of the input (bit 10 to 11 or bit 12 to 13) in the configuration register:

- Voltage measurement: Range of values 0x0000 to 0x7FFFF
- Temperature measurement: 1 LSB = 0.1°C
- Resistance measurement: 1 LSB = 1 Ω

Analog input (single)

This register indicates the analog input value of the voltage measurement.

Range of values: 0x0000 to 0x7FFFF

Counter

The configuration register must be set in order to set the correct counter modes. Counter 1 and counter 2 registers have different meanings for different modes.

- **Incremental encoder operation**
  If the reference input in the configuration register is enabled, then the module is a 16-bit ABR counter whose actual value is located in counter 1 (only LW) and the stored R-value in counter2 (functions as latch).
  The frequency of the signal to be measured can be a maximum of 30 kHz.
  If the reference input is not active, then it is a 32-bit AB incremental encoder counter input that should be read with counter 1 (LW and HW).
- **Event counter operation**
  If the counters are initialized as event counters in the configuration register, we get a 32-bit counter (counter 1) and a 16-bit counter (counter 2).

Period measurement

The measurement can be begin at the decreasing or increasing edge depending on the configuration register. The R mode bit must be 0. Measurement always occurs up to the next identical edge. The counter frequency can be set to one of 2 levels (4 MHz or 31.25 kHz) or with an external frequency.

The frequency of the signal to be measured can be a maximum of 100 kHz.

If an overflow of the continuous counter occurs during the period measurement (e.g. due to an incorrect counter frequency), this can be detected by setting bit 9 in the configuration register. The maximum value of the counter is limited to 0x7FFFFFFF, however. The error bit in the status register is acknowledged by resetting bit 9 of the configuration register.

Gate measurement

The measurement can be begin at the decreasing or increasing edge depending on the configuration register. The R mode bit must be 0. Measurement always occurs up to the next edge. The counter frequency can be set to one of two levels (4 MHz or 31.25 kHz) or with an external frequency.

The frequency of the signal to be measured can be a maximum of 100 kHz.

If an overflow of the continuous counter occurs during gate measurement (e.g. due to an incorrect counter frequency), this can be detected by setting bit 9 in the configuration word. The maximum value of the counter is limited to 0x7FFFFFFF, however. The error bit in the status word is acknowledged by resetting bit 9 of the configuration word.

Trigger value

This register contains the input value that caused the comparator to be triggered.

This value remains the same until the next time the comparator is triggered.

Trigger timestamp

This register contains the time at which the comparator was triggered (microseconds since the end of the last X2X cycle).

This value remains the same until the next time the comparator is triggered.

Module status

Bit	Description	Value	Information
0 - 3	Reserved	0	
4	Analog input 1	0	OK
		1	Error
...		...	
7	Analog input 4	0	OK
		1	Error
8	Comparator	0	Comparator has not been triggered
		1	Comparator has been triggered
9	Counter 1: Period or gate measurement	0	Valid value in the range 0 to 0x7FFFFFFF (only valid if bit 9 in the configuration register is set)
		1	Counter overflow (acknowledge by resetting bit 9 in the configuration register)
10	Reserved	0	
11	Monitoring of the module power supply	0	Voltage within warning limits (18 to 10 VDC)
		1	Voltage outside warning limits (18 to 10 VDC)
12	Monitoring of the power supply for digital inputs	0	OK
		1	Error
13	Summation current of 5 and 6	0	<4 A
		1	>4 A
14	Summation current of 7 and 8	0	<4 A
		1	>4 A
15	Monitoring of the output supply	0	OK
		1	Error

Digital outputs

This register is used to indicate the output status of the digital outputs.

As a result, the output with the lowest channel number is located in the LSB; the bits of the outputs that are not present are ignored by the module.

Bit	Name	Value	Information
0	Channel 1	0	Digital output reset
		1	Digital output set
...		...	
7	Channel 8	0	Digital output reset
		1	Digital output set

Analog output

This register indicates the initial state of digital outputs.

Range of values: 0x8001 to 0x7FFF

PWM period

The period can be set between 1 and 1000 ms. The decimal value 1000 corresponds to a period of 1 sec.

Pulse width

The pulse width (pulse width 1 and pulse width 2) can be set in 0.1% steps between 0% and 100%. The decimal value 1000 corresponds to a pulse width of 100%.

Module configuration

Bit	Description	Value	Information
0	Comparator function	0	Comparator function off
		1	Comparator function on[1)]
1	R mode	0	R mode for AB(R) counter off
		1	R mode for AB(R) counter on
2	Type of measurement	0	Period measurement
		1	Gate measurement
3	For period or gate measurement	0	Start measurement on rising edge
		1	Start measurement on falling edge
4 - 5	Counter mode	00	No counter operation
		01	AB(R) counter
		10	Event counter
		11	Counter 1: Period or gate measurement Counter 2: Event counter
6 - 7	Counter frequency	00	4 MHz
		01	31.25 kHz
		10	External counter frequency (digital input 3)
		11	Special mode[2)]
8	Active comparator output	0	Digital output 1
		1	Analog output 3
9	Overflow detection 1	0	Overflow detection off. Overflow bit from counter 1 is reset.
		1	Overflow detection of active counter 1 (value limited to 0x7FFFFFFF)
10 - 11	Analog input 1	00	Voltage measurement
		01	Temperature measurement PT1000
		10	Temperature measurement KTY10-6
		11	Resistance measurement 1 to 4000 Ω
12 - 13	Analog input 2	00	Voltage measurement
		01	Temperature measurement PT1000
		10	Temperature measurement KTY10-6
		11	Resistance measurement 1 to 4000 Ω
14	Trigger comparator	0	Comparator triggered when the value falls below the threshold value
		1	Comparator triggered when the value exceeds the threshold value
15	Time/Counter	0	Reset time/counter
		1	Time/counter switched on (set this bit to 1 after counter has been configured)

1) If the comparator has been triggered once, it retains its state until it is switched off and, if necessary, switched back on again.
2) Only valid for incremental encoder operation without R input: Time counter in µs (the time is temporarily saved and reset on every edge of the A or B signal.

Trigger level

This register contains the threshold value / trigger value for the comparator.

Comparator output

If the comparator is not switched on or has not been triggered, then the active comparator output is determined by the default output.

The active output is defined as follows when the comparator is triggered:

- **Analog active output** (bit 8 of the configuration register is 1):
  The register contains the value (0x8001 to 0x7FFF) output on analog output 3.
- **Digital active output** (bit 8 of the configuration register is 0):
  Bit 0 of this register is output on digital output 1.

7.6 ACOPOSmicro

7.6.1 80PS080X3.10-010

Register	Name	Bytes	Module	
			80PS080X3.10-01[1]	
Input:				
2	Status packed 01	2	Word	
83	**HI:** 0 **LO:** Voltage 01	2	Word	
86	Current 01	2	Word	
Output:				
3	Control packed 01	1		Byte
Data bytes in DP frame			6 in	1 out

1) Configuration registers can be modified in the parameter dialog box for the I/O module and are transferred asynchronously.

Support with firmware version ≥ V1.43

Status packed

This register contains status and error bits for the module.

Bit	Description	Value	Information
0	ErrorOutput01	0	No error
		1	The power output was shut off due to an error. After the error has been corrected and acknowledged, the power output can be enabled again. Possible causes of errors: • Short circuit (OverloadError01) • Overtemperature (StatusOvertemperature01) • Output voltage of the power output >100 V
1	OverloadError01	0	No error
		1	Short circuit or overload on the power output: • When a short circuit occurs, the output is switched off and can be enabled again by acknowledging the error. • When an overload occurs, the current is limited to 90% of the nominal current. Acknowledging the error allows overload operation to be re-enabled.
2	CurrentLimit01	0	Constant output voltage
		1	Current limiting active
3	StatusOvervoltage01	0	No error.
		1	Overvoltage on the power output. Voltage is 5 V higher than the chopper reference. No cutoff (not until 100 V).
4	StatusPhaseDetection01	0	No phase failure
		1	At least one phase failed. No more power is delivered to the power output.
5	StatusOvertemperature01	0	Temperature within permissible range (T < 75°C)
		1	Overtemperature error (T > 80°C). The power output is switched off and can be activated again by acknowledging the error.
6	ChopperActive01	0	Chopper inactive
		1	Chopper active
7	StatusBleeder01	0	No error: T < (TempLimitBleeder01 - 5°C)
		1	Temperature of the braking resistor exceeded: T > TempLimit-Bleeder01
8	StatusChopper01	0	No error: T < 75°C
		1	Temperature of the chopper output exceeded: T > 80°C
9	StatusOutput02	0	No error
		1	Short circuit or overload on power output. Output is switched off for 10 ms and then back on.
10 - 15	Reserved	-	

Voltage

Analog voltage measurement at the power output

Resolution: 1 V / Digit

Current

Analog current measurement at the power output

Resolution: 0.1 A / Digit

Control packed

This register contains the error acknowledgment bit.

Bit	Description	Value	Information
0	ClearError01	0	
		1	The rising edge of this bit acknowledges the following power output errors: • ErrorOutput01 • OverloadError01
1 - 7	Reserved	0	

7.6.2 80SD100XD.C044-01 / 80SD100XD.C0XX-01 / 80SD100XS.C0XX-01

Register	Name	Bytes	Module					
			80SD100XD. C044-01*1) 80SD100XD. C0XX-01*1) 80SD100XD.C033-01 80SD100XD.C011-01		80SD100XD. C044-01-C05 80SD100XD. C0XX-01-C05 80SD100XD.C033-01-C05 80SD100XD.C011-01-C05		80SD100XS. C0XX-01 80SD100XS. C0XX-C05* 80SD100XS. C04X-01* 80SD100XS. C04X-01-C05*	
Input:								
0	Actual position 1	4	Long		Long		Long	
4	Status word 1	2	Word		Word		Word	
6	Input status	1	Byte		Byte		Byte	
8	Actual position 2	4	Long		Long			
12	Status word 2	2	Word		Word			
Output:								
0	Position set and speed set 1	4		Long		Long		Long
4	Control word 1	2		Word		Word		Word
6	**HI:** Brake 1 **LO:** Mode 1 Mode	2		Word		Word		Word
8	Position set and speed set 2	4		Long		Long		
12	Control word 2	2		Word		Word		
14	**HI:** Brake 2 **LO:** Mode 2	2		Word		Word		
Data bytes in DP frame			13 in	16 out	13 in	16 out	7 in	8 out

1) Configuration registers can be modified in the parameter dialog box for the I/O module and are transferred asynchronously.

Module names with '*': Support with firmware version ≥ V1.43

Actual position

This synchronous register contains the current position of the internal position counter in microsteps.

On variants with an encoder, this register can be toggled to the current encoder position (see bit 14 in the Control word register).

Status word

The bits in the *status word* reflect the state of the state machine.

Bit	Description	Value	Information
0	Ready to switch on	0 or 1	
1	Switched on	0 or 1	
2	Operation enabled	0 or 1	
3	Fault (error bit)	0 or 1	
4	Voltage enabled	0 or 1	
5	Quick stop	0 or 1	
6	Switch on disabled	0 or 1	
7	Warning	0 or 1	
8	Reserved	-	
9	Remote	1	(always 1 since there is no local mode)
10	Target reached	0 or 1	This bit has one of the following meanings depending on the *mode*: ▪ Position reached ▪ Referencing complete ▪ Speed reached See also Extended control word.
11	Internal limit active	0	Current position within software limits.
		1	Software limit overflow or underflow
12	Setpoint acknowledge	-	See Extended control word.
13 - 15	Reserved	-	

Input status

This register indicates the logical states of digital inputs.

Bit	Description	Value	Information
0	Digital input 1	0 or 1	
1	Digital input 2	0 or 1	
2 - 7	Reserved	0	

Depending on the ACOPOSmicro variant, these digital inputs are used as a trigger input.

Position set and speed set

This synchronous register is used to set the position or speed depending on the operating mode (see section Mode).

- **Position mode:** Cyclic setting of the position setpoint in microsteps.
  In ramp mode, one microstep is always 1/256 of a full step.
- **Speed mode:** Cyclic setting of the speed setpoint (signed value).
  Unit: Microsteps/cycle

Control word

This register can be used to transmit commands based on the state of the module.

Bit	Description[1)]	Value	Information
0	Switch on	0 or 1	
1	Enable voltage	0 or 1	
2	Quick stop	0 or 1	
3	Enable operation	0 or 1	
4 - 6	See Extended control word.	-	
7	Fault reset	0 or 1	
8	See Extended control word.	-	
9 - 10	Reserved	0	(only permitted to be written to with 0)
11	Motor ID trigger[2)]	0	No effect
		1	Rising edge: Starts measurement of the motor ID.
12	Warning reset	0	No effect.
		1	Rising edge: Resets any warnings.
13	Undercurrent detection	0	Disables current error detection (default).
		1	Enables current error detection.
14	Contents of register *Current position (cyclic/acyclic)*[3)] (default: 0)	0	Cyclic: Internal position counter Acyclic: Encoder position
		1	Cyclic: Encoder position Acyclic: Internal position counter
15	Reserved	0	

1) Some bits are only available for certain variants.
2) This bit can be used to trigger a measurement of the motor ID. The application must ensure that the conditions for measurement are fulfilled.
3) This register is only available for variants where an encoder can be connected to the motor to detect the position.

Brake

Bit	Description	Value	Information
0	Controls "24 VDC brake output"	0	Brake output not set. Holding brake blocked (closed).
		1	Brake output set. The holding brake is released (open).
1 - 7	Reserved	0	

The *Motor break* register controls the module's brake output (X2/6: 24 VDC brake output).

On 2-channel variants, bit 0 of the two registers *Motor brake 1/2* are linked with an OR operator. This means that the brake output is set if the bit is set for one or both motors.

Mode

The operating mode determines the behavior of the drive. The following modes are available:

Value (dec.)	Description
0	No mode selected
1	Move to target position as soon as the target position is changed See also Extended control word.
2	Speed mode
-120	Set home position
-121	Remaining distance mode
-122	Set the actual position
-123	Move to target position
-124	Two-position mode
-125	Move to fixed position A
-126	Move to fixed position B
-127	Homing positive
-128	Homing negative

Information:

For all modes: Bit *Target reached* in Status word is set when the current action is ended (when the position or speed, depending on the mode, has been reached).

A new position or speed can be specified even before the current action is finished.

Extended control word

Information:

Some register descriptions in this overview contain only the description without an extended control word.

For a description of these registers with an extended control word, see the ACOPOSmicro user's manual.

7.7 ACOPOSinverter

7.7.1 ACPi_X64

X2X Link register	Bezeichnung	Bytes	Module	
			8I64xxxxxxx.00X-1-C05	
Input:				
2050	ETAD → Status word	2	Word	
2058	RFRD → Output speed	2	Word	
2066	ETI → Extended status word	2	Word	
2074	OTR → Motor torque	2	Word	
2082	LCR → Current in the motor	2	Word	
2090	THD → Drive thermal state	2	Word	
2098	THR → Motor thermal state	2	Word	
2106	ERRD → CiA402 fault code	2	Word	
2114	LFT → Last detected fault	2	Word	
2122	IOLR → Value of logic I/O	2	Word	
37	**HI:** 0 **LO:** StatusDigitalOutputPacked	1	Word	
Output:				
1	**HI:** reserved **LO:** DigitalOutputPacked	1		Word
2050 8999	CMD → Control word	2		Word
2058	LFRD → Speed setpoint	2		Word
2066	CMI → Extended control word	2		Word
2074	IOLR → Value of logic I/O	2		Word
Data bytes in DP frame			22 in	10 out

Support with firmware version ≥ V1.43

ETAD → Status word

Bit	Value	Description
0	1	Ready to switch on
1	1	Switched on
2	1	Operation enabled
3	0	No detected fault
	1	Malfunction, detected fault (FAI)
4	1	Voltage disabled (still equals 0)
5	1	Quick stop
6	1	Switch on disabled
7	0	No alarm
	1	Alarm present
8	-	Reserved
9	0	Forced local mode in progress (FLO)
	1	No forced local mode
10	0	Reference not reached (transient state)
	1	Reference reached (steady state)
11	0	LFRD reference normal
	1	LFRD reference exceeded (< LSP or > HSP) **LFRD is expressed in rpm, LSP and HSP in Hz**
12 - 13	-	Reserved
14	0	No stop imposed by STOP key on built-in keypad or on the remote display terminal
	1	Stop imposed by STOP key on built-in keypad or on the remote display terminal
15	0	Forward rotation (output frequency)
	1	Reverse rotation (output frequency)

RFRD → Output speed

Output speed

Unit: 1 rpm

ETI → Extended status word

Bit	Value	Description
0	0	Write parameters authorized
	1	Write parameters not authorized (the drive is in the process of saving the current parameters from the RAM to the EEPROM)
1	0	No parameter consistency check + drive locked on standstill
	1	Parameter consistency check
2	0	Fault state reset not authorized
	1	Fault state reset authorized
3	-	Reserved
4	0	Motor stopped
	1	Motor running
5	0	No DC injection
	1	DC injection
6	0	Drive in steady state
	1	Drive in transient state
7	0	No motor thermal overload alarm
	1	Motor thermal overload alarm
8	0	No alarm if excessive braking
	1	Alarm if excessive braking
9	0	Drive not accelerating
	1	Drive accelerating
10	0	Drive not decelerating
	1	Drive decelerating
11	0	No current limit alarm
	1	Current limit alarm
12	0	Fast stop not in progress
	1	Fast stop in progress
13 - 14	Bit 14 = 0 and bit 13 = 0	Drive controlled via terminal block or built-in keypad
	Bit 14 = 0 and bit 13 = 1	Drive controlled via the remote display terminal
	Bit 14 = 1 and bit 13 = 0	Drive controlled via ModBus
	Bit 14 = 1 and bit 13 = 1	Drive controlled via CanOpen
15	0	Forward rotation requested (reference)
	1	Reverse rotation requested (reference)

OTR → Motor torque

Motor torque

Value range: 0 to 100% in 1% steps

LCR → Current in the motor

Current in the motor

Unit: 0.1 A

THD → Drive thermal state

Drive thermal state

Unit: 1%

THR → Motor thermal state

Motor thermal state

Unit: 1%

ERRD → CiA402 fault code

Value		Description
16#0000	nOF	No fault code saved
16#1000	CrF	Capacitor pre-charge detected fault or
	OLF	Motor overload or
	SOF	Motor overspeed
16#2310	OCF	Overcurrent
16#2320	OCF	Impeding short-circuit or Power module, specific to 15kW drives
16#2330	SCF	Motor short-circuit (to ground)
16#2340	OCF	Motor short-circuit (phase to phase)
16#3110	OSF	Line supply overvoltage
16#3120	USF	Line supply undervoltage
16#3130	PHF	Line supply phase loss
16#3310	ObF	DC bus overvoltage or
	OPF	Motor phase loss or Motor phase loss - 3 phases
16#4210	OHF	Drive overheating
16#5520	EEF	EEPROM memory
16#6100	InF	Internal
16#6300	CFF	Incorrect configuration (parameters) or
	CFI	Invalid configuration (parameters)
16#7300	LFF	4 - 20 mA loss
16#7510	SLF	Modbus communication interruption
16#8100	COF	Communication interruption, line 2 (CANopen)
16#9000	EPF	External fault
16#FF00	tnF	Auto-tuning was unsuccessful
16#FF01	bLF	Brake control
16#7520	ILF	Optional internal link
16#7510	CNF	Communication interruption on the communication card

LFT → Last detected fault

Value		Description
0	"nOF"	No fault code saved
3	"CFF"	Incorrect configuration (parameters)
4	"CFI"	Invalid configuration (parameters)
5	"SLF"	Modbus communication interuption
6	"ILF"	Internal communcation interuption
7	"CnF"	Communication option card
8	"EPF"	External fault
9	"OCF"	Overcurrent
10	"CrF"	Capacitor pre-charge
13	"LFF"	4 - 20 mA loss
16	"OHF"	Drive overheating
17	"OLF"	Motor overload
18	"ObF"	DC bus overvoltage
19	"OSF"	Line supply overvoltage
20	"OPF"	Motor phase loss
21	"PHF"	Line phase loss
22	"USF"	Line supply undervoltage
23	"OCF"	Motor short-circuit (phase to phase)
24	"SOF"	Motor overspeed
25	"tnF"	Auto-tuning was unsuccessful
26	"IF1"	Unknown rating
27	"IF2"	MMI card
28	"IF3"	MMI communication
29	"IF4"	Industrial EEPROM
30	"EEF"	EEPROM memory
31	"OCF"	Impeding short-circuit
32	"SCF"	Motor short-circuit (to ground)
33	"OPF"	Motor phase loss - 3 phases
34	"COF"	Communication interuption, fault line 2 (CANopen)
35	"bLF"	Brake control
36	"OCF"	Power module, specific to 15kW drives
55	"SCF"	Power module or motor short-circuit, detected at power up.

IOLR → Value of logic I/O

Bit	Name	Value	Description
0	Value of logic input "LI1"	0	inactive
		1	active
1	Value of logic input "LI2"	0	inactive
		1	active
2	Value of logic input " LI3"	0	inactive
		1	active
3	Value of logic input " LI4"	0	inactive
		1	active
4	Value of logic input " LI5"	0	inactive
		1	active
5	Value of logic input " LI6"	0	inactive
		1	active
6	Reserved	-	
7	Keypad presence	0	absent
		1	present
8	Value of "R1" relay output, also accessible in write mode if R1 is not assigned	0	inactive
		1	active
9	Value of "R2" relay output, also accessible in write mode if R2 is not assigned	0	inactive
		1	active
10	Value of "LO" logic output, also accessible in write mode if LO is not assigned	0	inactive
		1	active
11 - 13	Reserved	-	
14	AOC/AOV	0	logic output
		1	analog output
15	Reserved	-	

StatusDigitalOutputPacked

Bit			
0	Status of digital output	0	is OK
		1	is not OK
1 - 7	Reserved	-	

DigitalOutputPacked

Bit			
0	Digital output	0	Disable
		1	Enable
1 - 7	Reserved	-	

CMD → Control word

0	Switch on	0	inactive
		1	active
1	Disable Voltage	0	active
		1	inactive
2	Quick Stop	0	active
		1	inactive
3	Enable Operation	0	inactive
		1	active
4 - 6	Reserved	0	
7	Fault state reset	-	active on rising edge 0 → 1
8 - 10	Reserved	0	
For "Access level" LAC (page 35) = L1 or L2:			
11	Direction	0	Forward direction command
		1	Reverse direction command
12	Stop command	0	No action
		1	Stop command depending on the Stt "Stop type" parameter
13	Injection stop	0	No action
		1	Injection stop command
14	Fast stop	0	No action
		1	Fast stop command
15	Reserved	0	
For "Access level" LAC (page 35) = L3:			
11	Direction	0	Forward direction command
		1	Reverse direction command
12	Stop command	0	No action
		1	Stop command depending on the Stt "Stop type" parameter
13 - 15	No action	-	

Bits 11 to 15 can be assigned to the following functions:

- Ramp switching (rPS)
- Fast stop (FSt)
- DC injection (DCI)
- 2 preset speeds (PS2)
- 4 preset speeds (PS4)
- 8 preset speeds (PS8)
- 16 preset speeds (PS16)
- 2 preset PI references (Pr2)
- 4 preset PI references (Pr4)
- Switching for 2nd current limit (LC2)
- Switching, motor 2 (CHP)
- External fault (EtF)

For example, to use bit 15 to switch the ramp, simply set the "Ramp switching" rPS configuration parameter (page 39) to Cd15.

LFRD → Speed setpoint

Speed setpoint

Unit: 1 rpm; Factory setting: 0 rpm

CMI → Extended control word

0	1)	0	No action
		1	Recall factory settings command
1	2)	0	No action
		1	Save configuration/adjustments in EEPROM
2	Reserved	-	
3	External fault behaviour	0	No action
		1	External fault. The drive's behaviour during an external fault is defined by parameter EPL.
4	Ramp	0	No action
		1	Ramp switching command
5 - 8	Reserved	-	
9	Resolution	0	Normal resolution (references, output speed and output frequency in physical units: rpm and Hz)
		1	High resolution (references, output speed and output frequency in 32767 points for 600 Hz)
10 - 12	Reserved	-	
13	Lock Drive	0	Drive not locked on standstill
		1	Drive locked on standstill
14	Modbus communication	0	Control with Modbus communication monitoring
		1	Control with no Modbus communication monitoring (NTO)
15	Parameter consistency	0	Parameter consistency check
		1	No parameter consistency check + drive locked on standstill (switching this bit to 0 will revalidate all parameters)

1) This bit automatically resets to 0 when the request is taken into account. It is only active when the drive has come to a complete stop: ETI.4 = ETI.5 = 0.
2) If voltage is sufficient (no USF detected fault). This bit automatically resets to 0 when the request is taken into account. During saving (ETI.0 = 1), parameters cannot be written.