

# X20DO2321

## 1 General information

The module is equipped with 2 outputs for 3-wire connections. It is designed for X20 6-pin terminal blocks. If needed (e.g. for logistical reasons), the 12-pin terminal block can also be used.

- 2 digital outputs
- Sink connection
- 3-wire connections
- 24 VDC and GND for actuator supply
- Integrated output protection
- OSP mode

## 2 Order data


Model number	Short description	Figure
	<b>Digital outputs</b>	
X20DO2321	X20 digital output module, 2 outputs, 24 VDC, 0.5 A, sink, 3-wire connections	
	<b>Required accessories</b>	
	<b>Bus modules</b>	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O supply continuous	
	<b>Terminal blocks</b>	
X20TB06	X20 terminal block, 6-pin, 24 VDC keyed	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 1: X20DO2321 - Order data

### 3 Technical data

Model number	X20DO2321
Short description	
I/O module	2 digital outputs 24 VDC for 3-wire connections
General information	
B&R ID code	0x22B3
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Outputs	Yes, using status LED and software (output error status)
Power consumption	
Bus	0.13 W
Internal I/O	0.3 W
Additional power dissipation caused by actuators (resistive) [W] <sup>1)</sup>	+0.06
Certifications	
CE	Yes
KC	Yes
EAC	Yes
UL	cULus E115267 Industrial control equipment
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÜ 09 ATEX 0083X
Digital outputs	
Variant	FET negative switching
Nominal voltage	24 VDC
Switching voltage	24 VDC -15 % / +20 %
Nominal output current	0.5 A
Total nominal current	1 A
Connection type	3-wire connections
Output circuit	Sink
Output protection	Thermal cutoff if overcurrent or short circuit occurs (see value "Peak short circuit current") Internal inverse diode for switching inductive loads (see section "Switching inductive loads")
Actuator power supply	0.5 A in total for output-independent actuator supply
Diagnostic status	Output monitoring with 10 ms delay
Leakage current when switched off	75 µA
R <sub>DS(on)</sub>	120 mΩ
Peak short-circuit current	<7 A
Switch-on in the event of overload shutdown or short-circuit shutdown	Approx. 10 ms (depends on the module temperature)
Switching delay	
0 → 1	<300 µs
1 → 0	<300 µs
Switching frequency	
Resistive load	Max. 500 Hz
Inductive load	See section "Switching inductive loads"
Braking voltage when switching off inductive loads	Typ. 50 VDC
Isolation voltage between channel and bus	500 V <sub>eff</sub>
Actuator power supply	
Voltage	Module supply minus voltage drop for short circuit protection
Voltage drop for short-circuit protection at 500 mA	Max. 2 V
Short-circuit proof	Yes
Power consumption	
Actuator power supply	Max. 12 W <sup>2)</sup>
Electrical properties	
Electrical isolation	Channel isolated from bus Channel not isolated from channel
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation elevation above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
Degree of protection per EN 60529	IP20

Table 2: X20DO2321 - Technical data


<b>Model number</b>	<b>X20DO2321</b>
<b>Ambient conditions</b>	
Temperature	
Operation	
Horizontal mounting orientation	-25 to 60°C
Vertical mounting orientation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
<b>Mechanical properties</b>	
Note	Order 1x X20TB06 or X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	12.5 <sup>+0.2</sup> mm

Table 2: X20DO2321 - Technical data

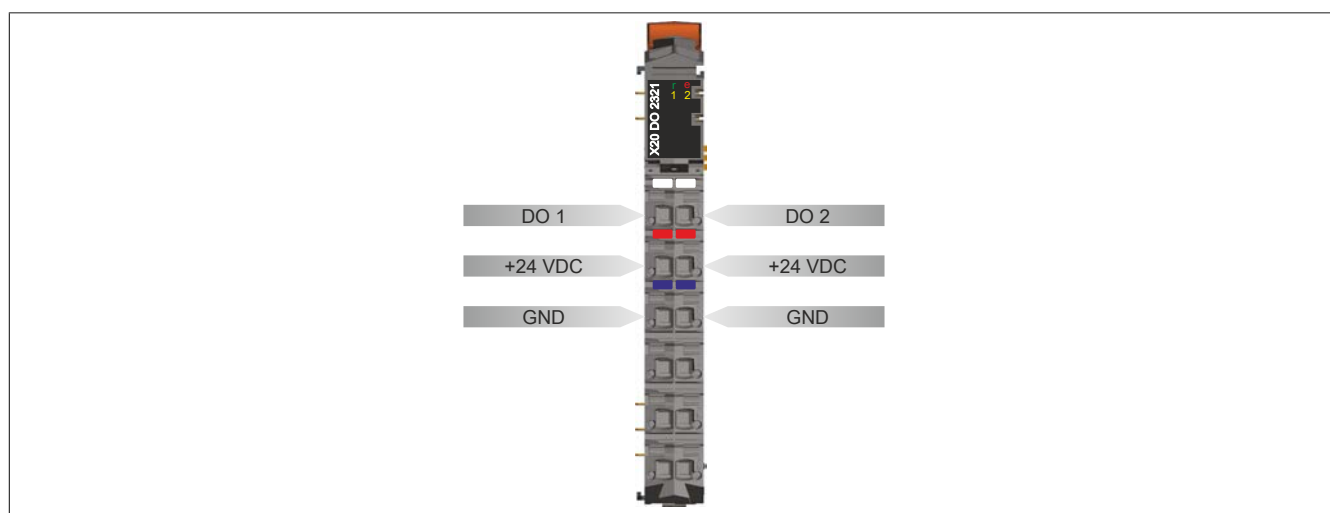
- 1) Number of outputs x  $R_{DS(on)}$  x Nominal output current<sup>2</sup>. For a calculation example, see section "Mechanical and electrical configuration" of the X20 system user's manual.
- 2) The power consumption of the sensors connected to the module is not permitted to exceed 12 W.

## 4 Status LEDs

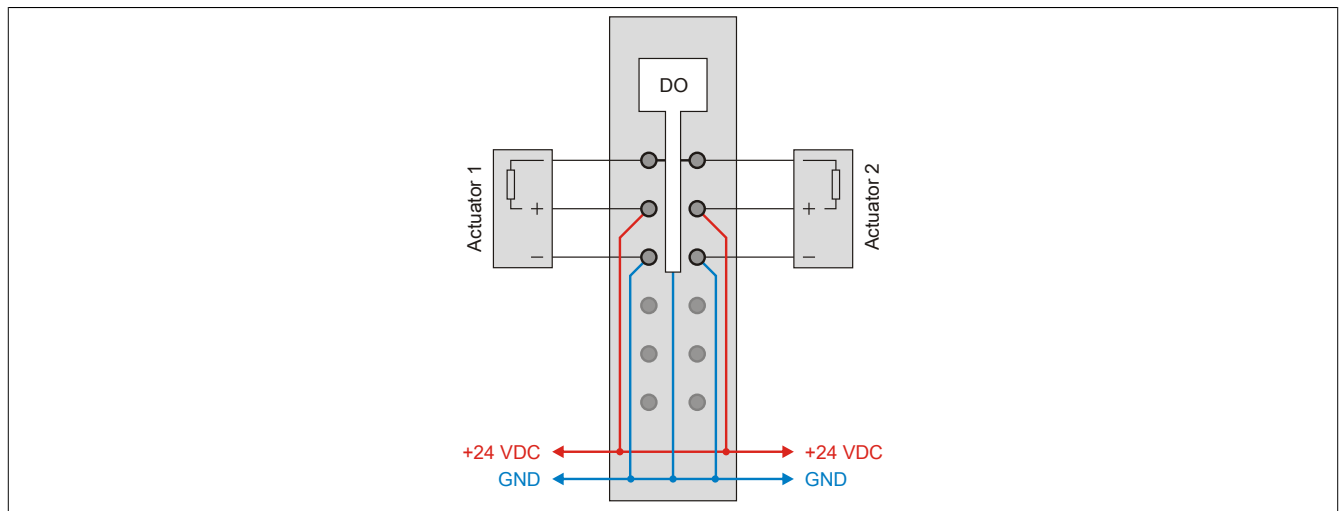
For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" of the X20 system user's manual.

Figure	LED	Color	Status	Description
	r	Green	Off	Module supply not connected
			Single flash	Reset mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
			Flickering (approx. 10 Hz)	The module is in the OSP state.
	e	Red	Off	Module supply not connected or everything OK
			Single flash	Warning/Error on an I/O channel. Level monitoring for digital outputs has been triggered.
	e + r	Red on / Green single flash		Invalid firmware
	1 - 2	Orange		Output status of the corresponding digital output

## 5 Pinout



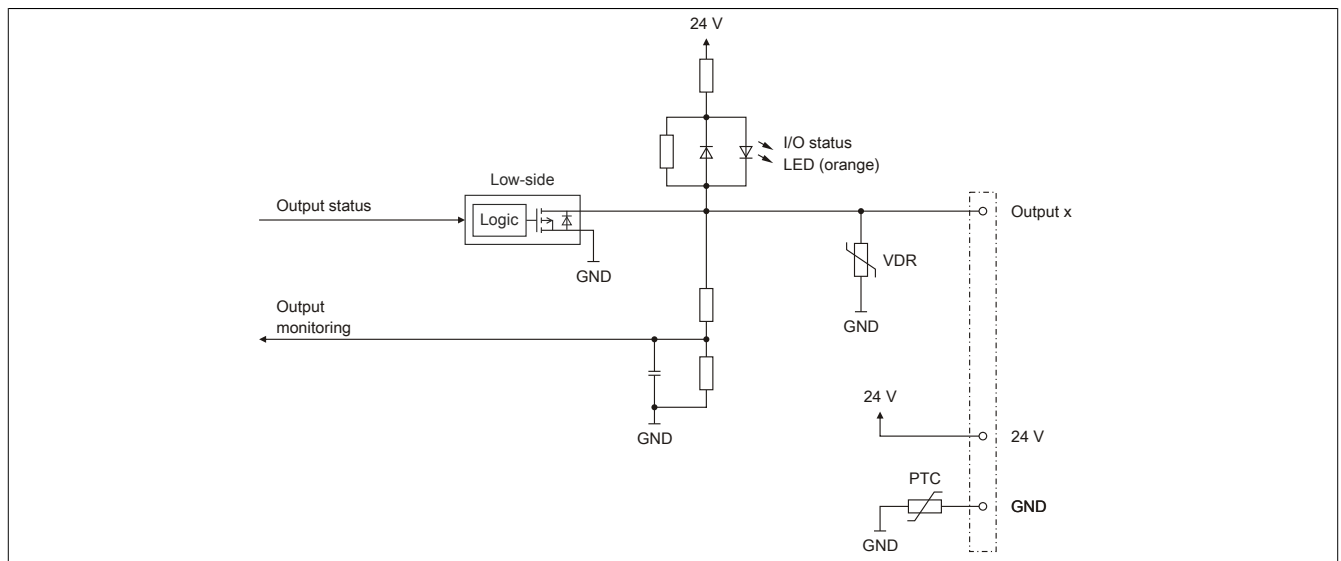
## 6 Connection example



## 7 OSP hardware requirements

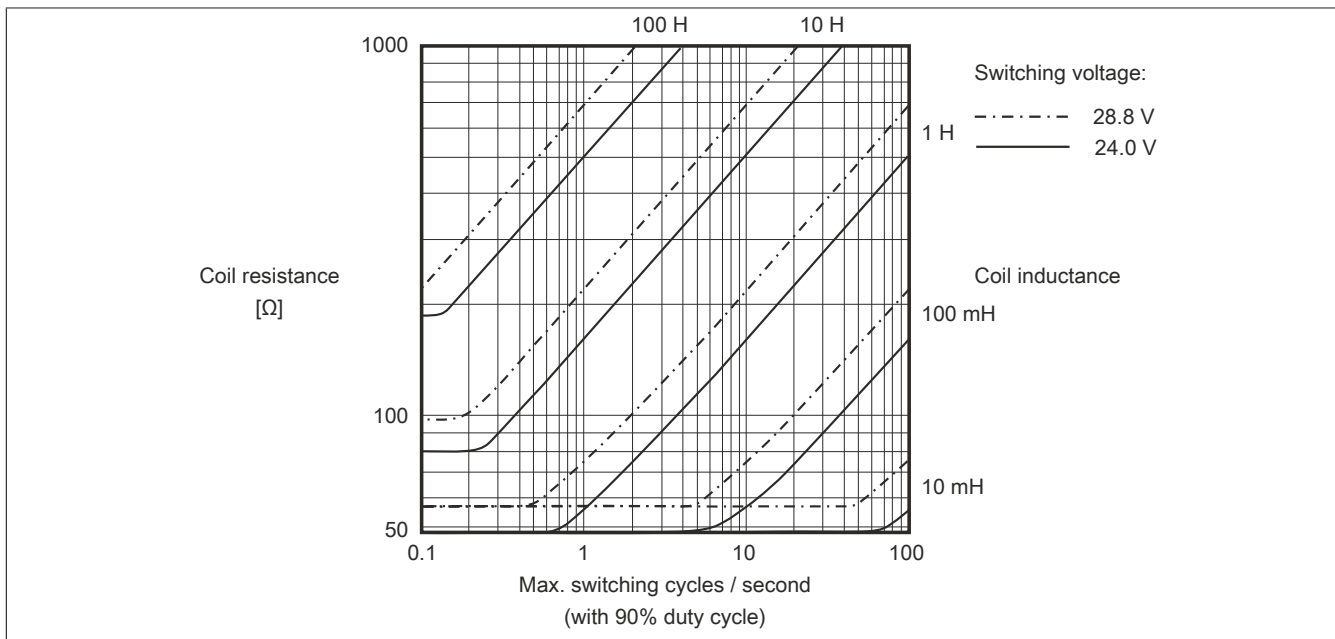
In order to use OSP mode sensibly, it should be ensured that the power supply of the output module and CPU are independent of each other when the application is set up.

## 8 Output circuit diagram



## 9 Switching inductive loads

Environmental temperature: 60°C, all outputs with the same load



### Information:

If the maximum number of operating cycles per second is exceeded, an external inverse diode must be used.

Operating conditions outside of the area in the diagram are not permitted!

## 10 Register description

### 10.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" of the X20 system user's manual.

### 10.2 Function model 0 - Standard

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	DigitalOutput	USINT			•	
		DigitalOutput01	Bit 0				
		DigitalOutput02	Bit 1				
30	1	StatusInput01	USINT	•			
		StatusDigitalOutput01	Bit 0				
		StatusDigitalOutput02	Bit 1				

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

### 10.3 Function model 1 - OSP

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	Switching state of digital outputs 1 to 2	USINT			•	
		DigitalOutput01	Bit 0				
		DigitalOutput02	Bit 1				
30	1	Status of digital outputs 1 to 2	USINT	•			
		StatusDigitalOutput01	Bit 0				
		StatusDigitalOutput02	Bit 1				
34	1	Enabling OPS output in the module	USINT			•	
		OSPValid	Bit 0				
32	-	CfgOSPMODE	USINT				•
36	-	CfgOSPValue	USINT				•

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

### 10.4 Function model 254 - Bus Controller

Register	Offset <sup>1)</sup>	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	Switching state of digital outputs 1 to 2	USINT			•	
		DigitalOutput01	Bit 0				
		DigitalOutput02	Bit 1				
30	-	Status of digital outputs 1 to 2	USINT		•		
		StatusDigitalOutput01	Bit 0				
		StatusDigitalOutput02	Bit 1				

1) The offset specifies where the register is within the CAN object.

#### 10.4.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use additional registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" of the X20 user's manual (version 3.50 or later).

#### 10.4.2 CAN I/O bus controller

The module occupies 1 digital logical slot on CAN I/O.

## 10.5 Digital outputs

The output status is transferred to the output channels with a fixed offset (<60 µs) based on the network cycle (SyncOut).

### 10.5.1 Switching state of digital outputs 1 to 2

Name:

DigitalOutput

DigitalOutput01 to DigitalOutput02

This register is used to store the switching state of digital outputs 1 to 2.

Only function model 0 - Standard:

Setting "Packed outputs" in the Automation Studio I/O configuration determines whether all bits of this register should be applied individually as data points in the Automation Studio I/O assignment ("DigitalOutput01" to "DigitalOutput0x") or whether this register should be displayed as a single USINT data point ("DigitalOutput").

Data type	Value	Information
USINT	0 to 3	Packed outputs = On
	See the bit structure.	Packed outputs = Off or function model ≠ 0 - Standard.

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput01	0	Digital output 01 reset
		1	Digital output 01 set
1	DigitalOutput02	0	Digital output 02 reset
		1	Digital output 02 set

## 10.6 Monitoring status of the digital outputs

On the module, the output states of the outputs are compared to the target states. The control of the output driver is used for the target state.

A change in the output state resets monitoring for that output. The status of each individual channel can be read. A change in the monitoring status generates an error message.

### 10.6.1 Status of digital outputs 1 to 2

Name:

StatusInput01

StatusDigitalOutput01 to StatusDigitalOutput02

The status of digital outputs 1 to 2 is mapped in this register.

Only function model 0 - Standard:

Setting "Packed outputs" in the Automation Studio I/O configuration determines whether all bits of this register should be applied individually as data points in the Automation Studio I/O assignment ("StatusDigitalOutput01" to "StatusDigitalOutput0x") or whether this register should be displayed as a single USINT data point ("StatusInput01").

Data type	Value	Information
USINT	0 to 3	Packed outputs = On
	See the bit structure.	Packed outputs = Off or function model ≠ 0 - Standard.

Bit structure:

Bit	Name	Value	Information
0	StatusDigitalOutput01	0	Channel 01: No error
		1	Channel 01: <ul style="list-style-type: none"> <li>Short circuit or overload</li> <li>Channel switched on and missing I/O power supply</li> <li>Channel switched off and external voltage applied on channel</li> </ul>
1	StatusDigitalOutput02	0	Channel 02: No error
		1	Channel 02: For error description, see channel 01

## 10.7 Function model "OSP"

In function model "OSP" (Operator Set Predefined), the user defines an analog value or digital pattern. This OSP value is output as soon as the communication between the module and master is aborted.

### Functionality

The user has the choice between 2 OSP modes:

- Retain last valid value
- Replace with static value

In the first case, the module retains the last value recognized as a valid output status.

When selecting mode "Replace with static value", a plausible output value must be entered in the associated value register. When an OSP event occurs, this value is output instead of the value currently requested by the task.

### 10.7.1 Enabling OPS output in the module

Name:

OSPValid

This data point makes it possible to start the output of the module and request the use of OSP during operation.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	OSPValid	0	Request OSP operation (after initial startup or module in stand-by)
		1	Request normal operation
1 - 7	Reserved	0	

Bit OSPValid exists once on the module and is managed by the user task. It must be set to start the enabled channels. As long as bit OSPValid remains set in the module, the module behaves the same as in function model "Standard".

If an OSP event occurs, e.g. communication between the module and master CPU aborted, then bit OSPValid is reset on the module. The module enters the OSP state and output occurs according to the configuration in register "OSPMoDe" on page 9.

**The following generally applies:**

**Even after regeneration of the communication channel, the OSP replacement value is still pending. The OSP state is only exited again when a set OSPValid bit is transferred.**

**When the master CPU is restarted, bit OSPValid bit is reinitialized in the master CPU. It must be set once more by the application and transferred via the bus.**

**In the event of brief communication errors between the module and master CPU( e.g. due to EMC), the cyclic registers fail to refresh for several bus cycles. Within the module, bit OSPValid is reset; the set bit is retained in the CPU, however. During the next successful transfer, the module-internal OSPValid bit is set again and the module automatically returns to normal operation.**

If the task in the master CPU needs the information about which output mode the module is currently in, bit ModulOK can be evaluated.

### Warning!

**If bit OSPValid bit is reset to "0" by the module, the output status no longer depends on the responsible task in the master CPU. Nevertheless, output is made depending on the configuration of the OSP replacement value.**



### 10.7.2 Setting OSP mode

Name:  
CfgOSPMode

This register controls the behavior of a channel when using OSP.

Data type	Values	Explanation
USINT	0	Replace with static value
	1	Retain last valid value

### 10.7.3 Defining an OSP-digital output value

Name:  
CfgOSPValue

This register contains the digital output value that is output in "Replace with static value" mode during OSP operation.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0		0 or 1	OSP output value for channel DigitalOutput00
...		...	
x		0 or 1	OSP output value for channel DigitalOutput0x

## Warning!

"OSPValue" is only applied by the module if bit "OSPValid" has been set in the module.

### 10.8 Minimum cycle time

The minimum cycle time specifies the time up to which the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
100 µs

### 10.9 Minimum I/O update time

The minimum I/O update time specifies how far the bus cycle can be reduced so that an I/O update is performed in each cycle.

Minimum I/O update time
Equal to the minimum cycle time