X20DO4613

1 General information

The module is a digital output module that is equipped with 4 opto-triac outputs using phase-angle control. L and N are fed to the module for zero-crossing detection.

The 4 outputs are electrically isolated from one another and are used for controlling external power triacs or non-parallel thyristors.

- 4 digital outputs
- Controls external power triacs or non-parallel thyristors
- Outputs with 48 - 240 VAC
- 50 Hz or 60 Hz
- Outputs electrically isolated from one another
- Phase-angle control
- Zero-crossing detection
- Negative half-waves can be switched off
- 2-wire connections
- 240 V coding
- OSP mode
- Frequency mode

Danger!

Risk of electric shock!

The terminal block is only permitted to conduct voltage when it is connected. It is not permitted to be disconnected or connected while voltage is applied or have voltage applied to it while it is removed under any circumstances.

This module is not permitted to be the last module connected on the X2X Link network. At least one subsequent X20ZF dummy module must provide protection against contact.

2 Order data

Model number	Short description	Figure
	Digital outputs	
X20DO4613	X20 digital output module, 4 triac coupler outputs, 48 to 240 VAC, 50 mA, zero-crossing detection, 240 V keyed	
	Required accessories	
	Bus modules	
X20BM12	X20 bus module, 240 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB32	X20 terminal block, 12-pin, 240 VAC keyed	

Table 1: X20DO4613 - Order data

3 Technical data

Model number	X20DO4613
Short description	
I/O module	4 digital outputs for controlling external power triacs or non-parallel thyristors
General information	
B&R ID code	0xAD05
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using LED status indicator and software
Outputs	Yes, using LED status indicator
Power consumption	
Bus	0.8 W
Internal I/O	-
External I/O	-
Additional power dissipation caused by actuators (resistive) [W] [1)]	+1 W
Certifications	
CE	Yes
KC	Yes
EAC	Yes
UL	cULus E115267 Industrial control equipment
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X
Digital outputs	
Variant	Opto-triac
Wiring	Normally open contact
Nominal voltage	48 to 240 VAC
Max. voltage	264 VAC
Rated frequency	47 to 63 Hz
Nominal current at 25°C	
Nominal output current	80 mA
Total nominal current	320 mA
Current over entire temperature range	
Output current	50 mA
Summation current	200 mA
Connection type	2-wire connections
Zero-crossing detection	Yes
Holding current	Max. 3.5 mA
Leakage current	Max. 1.5 mA (per channel)
Residual voltage (on-state voltage)	Max. 3 V
Phase-angle control	
Area	5 to 95%
Resolution	1%
Accuracy (60 to 240 VAC)	<100 µs
Voltage monitoring L - N	No
Recommended wiring	Twisted pair cabling to the terminal pairs
Line length	Max. 10 m
Overvoltage protection between L and N	Yes
Isolation voltages	
Channel - Bus	Tested at 2300 VAC
Channel - Channel	Tested at 2300 VAC
Protective circuit	
External	Generally fuse
Internal	Snubber circuit (RC element) and varistor
Electrical properties	
Electrical isolation	Channel isolated from channel and bus
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation elevation above sea level	
0 to 2000 m	No limitation
>2000 m	Not permitted
Degree of protection per EN 60529	IP20

Table 2: X20DO4613 - Technical data

Model number	X20DO4613
Ambient conditions	
Temperature	
Operation	
Horizontal mounting orientation	-25 to 60°C
Vertical mounting orientation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical properties	
Note	Order 1x terminal block X20TB32 separately. Order 1x bus module X20BM12 separately.
Spacing	12.5 $^{+0.2}$ mm

Table 2: X20DO4613 - Technical data

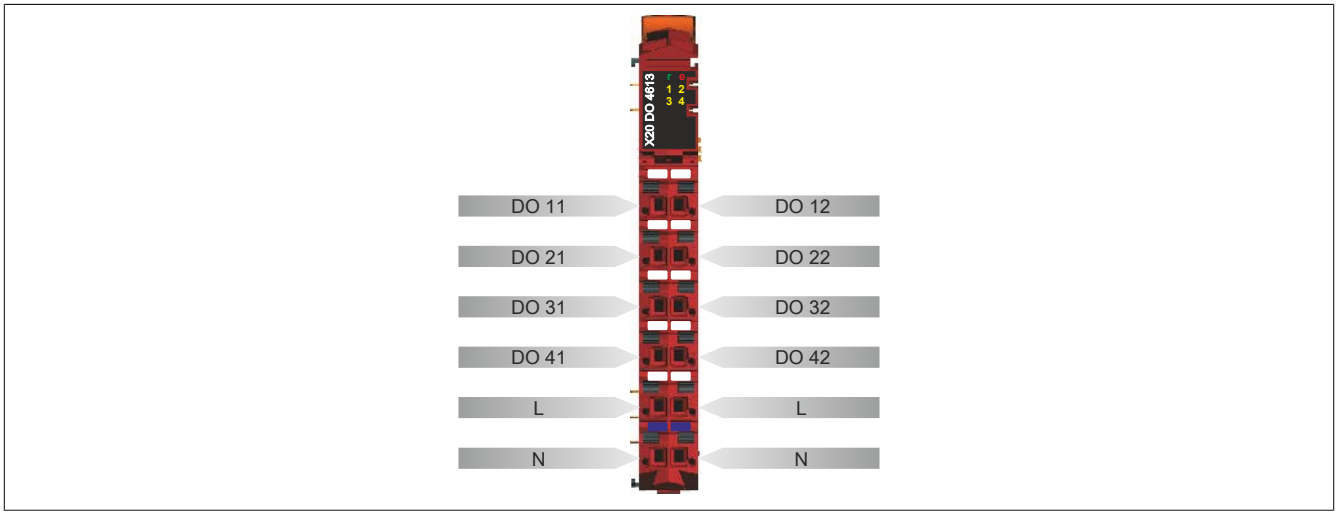
1) Number of outputs x Residual voltage (on-state voltage) x Nominal output current. For a calculation example, see section "Mechanical and electrical configuration" of the X20 system user's manual.

4 Status LEDs

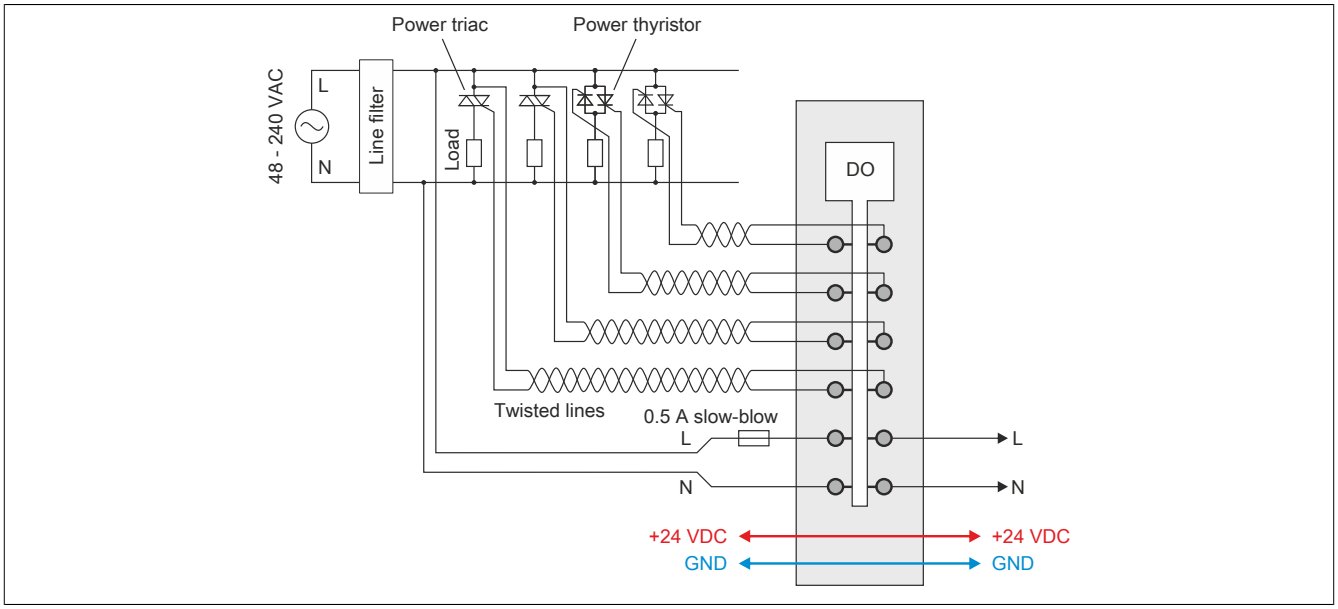
For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" of the X20 system user's manual.

Figure	LED	Color	Status	Description
	r	Green	Off	Module supply not connected
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
			Flickering (approx. 10 Hz)	Module is in OSP state
	e	Red	Off	Module supply not connected or everything OK
			On	Error or reset status
			Single flash	Loss of zero-crossing signal (input voltage absent or too low)
	e + r	Red on / Green single flash		Invalid firmware
	1 - 4	Orange		Control status of the corresponding digital output

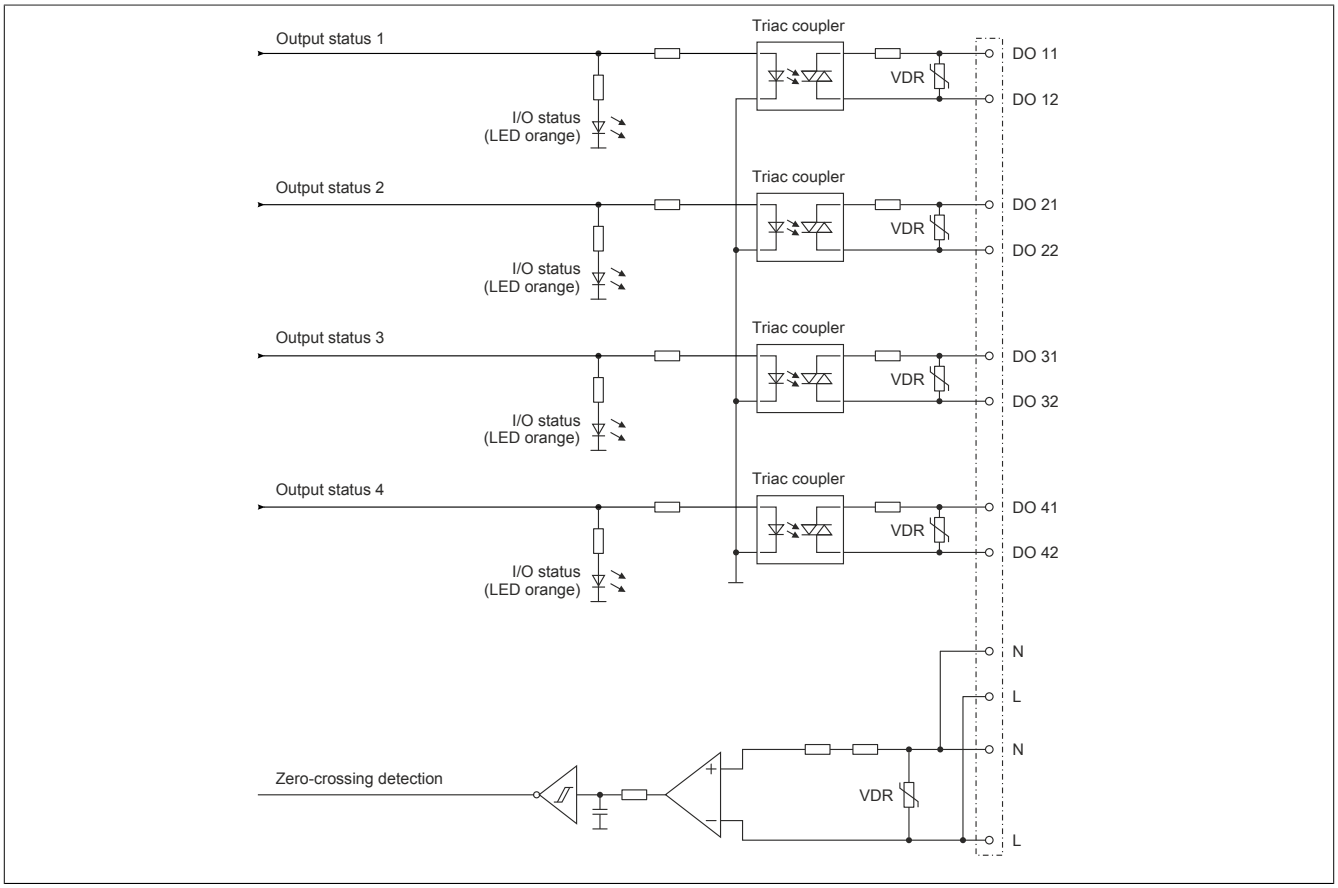
5 Pinout



6 Connection example



7 Output circuit diagram



8 Operating principle

The digital output module DO4613 was designed to control external triacs and thyristors.

The module is equipped with internal zero-crossing detection. Zero-crossing detection is the basis for a software PLL that generates 200 times the zero-crossing frequency. The output signal of the PLL is the base timer for the 4 PWM outputs in both digital and analog mode.

Upon detection of lost periods or periods that are too short, control to the outputs is cut until the PLL is tuned correctly. The tuning procedure can take several seconds. In addition, the "ZeroCrossingStatus" bit is set and the error LED enabled (valid frequency range for the supply is 47 to 63 Hz).

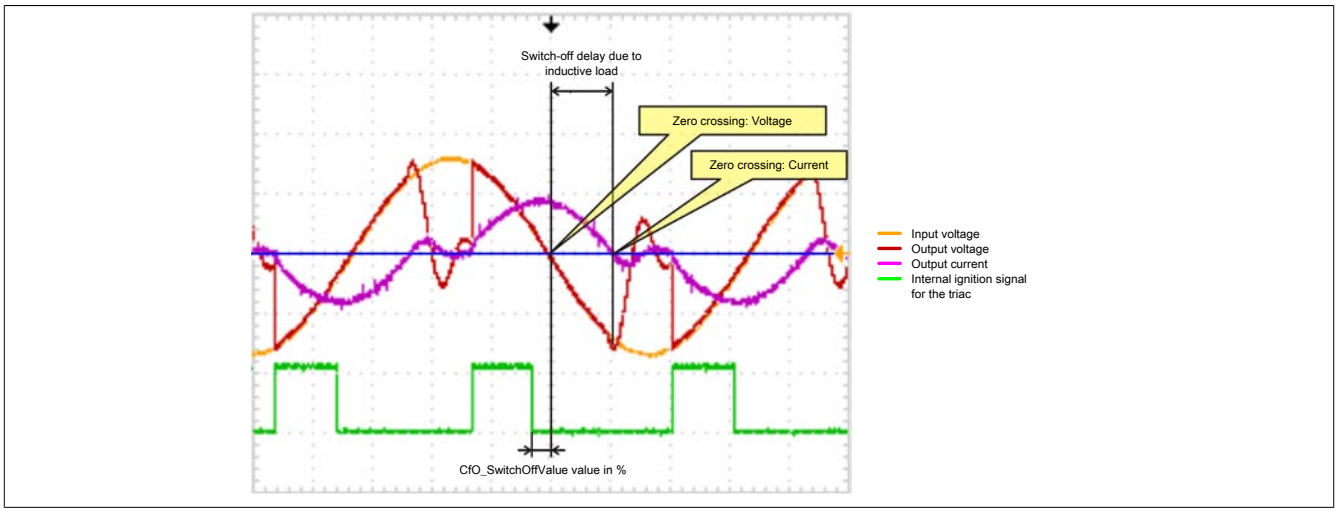
Information:

The jitter of the output signals generated by the PLL and communication can reach 0.5%.

9 Operation with inductive loads

As inherent to its functional principal, the triac output is cleared when the current crosses zero. Because zero crossing for current is delayed with inductive loads, it is possible that the triac will be fired again even though it is not completely cleared at higher output values (between 50 and 100% depending on the inductance of the load). In this case, a full-wave is output. This causes the available control range to be reduced (0 to 100%).

For control beyond the point of full-wave control (up to 100%), the value that is physically output no longer changes. However, this does not cause damage to the module.



10 Register description

10.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" of the X20 system user's manual.

10.2 Function model 0 - Standard and Function model 2 - Frequency mode

The only difference between function model 2 and function model 0 is the possibility of generating half-wave patterns in various frequencies. Register 18 "CfO_Frequency" is an additional register for this.

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Configuration - General						
2 + N * 2	AnalogOutput0N (Index N = 1 to 4)	USINT			•	
18	CfO_Frequency	UINT				•
18 + N * 2	ConfigOutput0N (Index N = 1 to 4)	USINT				•
28	ConfigOutput05	USINT				•
29	CfO_OutputTolerance	USINT				•
Communication						
2	DigitalOutput	USINT			•	
	DigitalOutput01	Bit 0				
	...	...				
	DigitalOutput04	Bit 3				
30	StatusInput01	USINT	•			
	ZeroCrossingInput	Bit 4				
	ZeroCrossingStatus	Bit 7				

10.3 Function model 1 - OSP

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Configuration - General						
2 + N * 2	AnalogOutput0N (Index N = 1 to 4)	USINT			•	
18 + N * 2	ConfigOutput0N (Index N = 1 to 4)	USINT				•
28	ConfigOutput05	USINT				•
29	CfO_OutputTolerance	USINT				•
Configuration - OSP						
34	Enabling OPS output in the module	USINT			•	
	OSPValid	Bit 0				
32	CfgOSPMode	USINT				•
36	CfgOSPValue	USINT				•
36 + N * 2	CfgOSPValue0N (Index N = 1 to 4)	USINT				•
Communication						
2	Switching state of digital outputs 1 to 4	USINT			•	
	DigitalOutput01	Bit 0				
	...	...				
	DigitalOutput04	Bit 3				
30	Status of the outputs	USINT	•			
	ZeroCrossingInput	Bit 4				
	ZeroCrossingStatus	Bit 7				

10.4 Function model 254 - Bus controller

Register	Offset	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
Configuration - General							
2 + N * 2	(N-1) * 2	AnalogOutput0N (Index N = 1 to 4)	USINT			•	
18 + N * 2	-	ConfigOutput0N (Index N = 1 to 4)	USINT				•
28	-	ConfigOutput05	USINT				•
29	-	CfO_OutputTolerance	USINT				•
Communication							
30	0	Status of the outputs	USINT	•			
		ZeroCrossingInput	Bit 4				
		ZeroCrossingStatus	Bit 7				

1) The offset specifies the position of the register within the CAN object.

10.4.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use additional registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" of the X20 user's manual (version 3.50 or later).

10.4.2 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN I/O.

10.5 General information

The digital output module was designed for phase control of resistive and inductive loads.

The module is equipped with internal zero-crossing detection. Zero crossing detection is the basis for a software PLL that generates 200 times the zero crossing frequency. The output signal of the PLL is the base timer for the 2 PWM outputs in both digital and analog mode.

Upon detection of lost periods or periods that are too short, control of the outputs is cut until the PLL is tuned correctly (can take several seconds). In addition, the "ZeroCrossingStatus" bit is set and the Error LED is enabled (valid frequency range for the supply is 45 to 65 Hz).

Information:

The jitter of the output signals generated by the PLL and communication can reach 0.5%.

10.6 Digital outputs

The output state of the outputs defined as digital is transferred to the output ports of the control switch in sync with the connected power mains. The switch-on state is applied when the voltage crosses zero on the positive half-wave and the switch-off state at the zero crossing for current in each half wave.

10.6.1 Switching state of digital outputs 1 to 4

Name:
DigitalOutput
DigitalOutput01 to DigitalOutput04

This register is used to store the switching state of digital outputs 1 to 4.

Only function model 0 - Standard:

Setting "Packed outputs" in the Automation Studio I/O configuration determines whether all bits of this register should be applied individually as data points in the Automation Studio I/O assignment ("DigitalOutput01" to "DigitalOutput0x") or whether this register should be displayed as a single USINT data point ("DigitalOutput").

Data type	Values	Information
USINT	0 to 15	Packed outputs = On
	See the bit structure.	Packed outputs = Off or function model ≠ 0 - Standard.

Bit structure:

Bit	Description	Value	Information
0	DigitalOutput01	0	Digital output 01 reset
		1	Digital output 01 set
...		...	
3	DigitalOutput04	0	Digital output 04 reset
		1	Digital output 04 set

Information:

The states in these registers are only applied when the channels are set to DIGITAL in register "ConfigOutput05" on page 10.

When using setting "Packed outputs", ALL channels must be set to DIGITAL. Mixed operation is not possible.

10.7 Analog outputs

The output value of the outputs defined as analog outputs (unit percent) is switched through to the control ports in sync with power mains. The analog value is output to the TRIAC control port in the range between (output value > SwitchOffValue) and (output value <= 95%) with a resolution of 1%.

Changes to the output value are applied at the next positive half-wave

10.7.1 Commutation angle for analog outputs 1 - 4

Name:
AnalogOutput01 to AnalogOutput04

These registers are used to set the commutation angle for phase angle control.

Values between 0 and 100 correspond to the output value for the respective channel in percent. Values above 100 correspond to 100%.

Data type	Value
USINT	0 to 100

Information:

The commutation angle for phase angle control set in these registers are only applied when the channels are set to ANALOG in register "ConfigOutput05" on page 10.

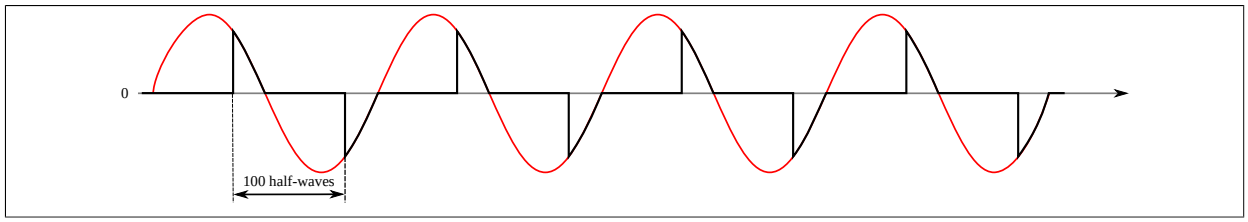
10.8 Output configuration

10.8.1 Configuring the half-wave pattern

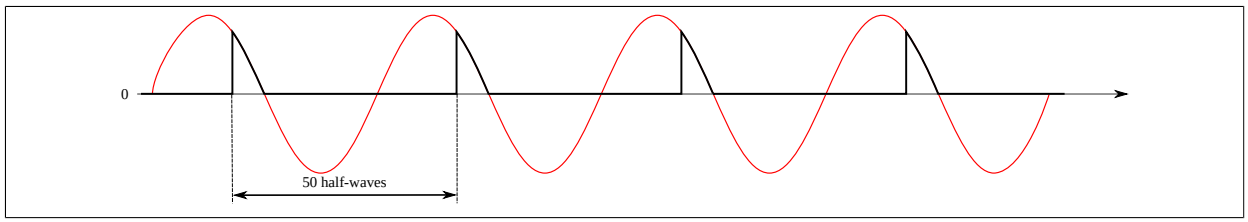
Name:
CfO_Frequency

This register can only be used in function model 2 - Frequency mode and makes it possible to configure the output of half-wave patterns in various frequencies. The commutation angle of the outputs is not affected by this. The following frequency patterns can be configured:

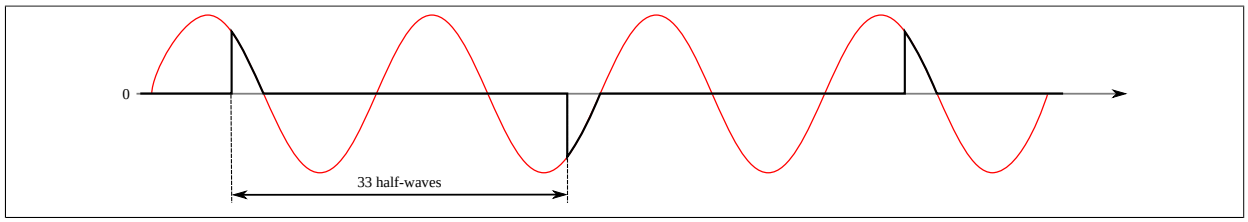
- 100 half-waves



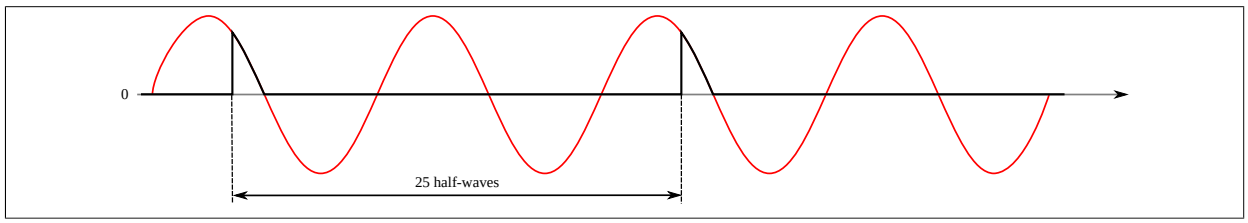
- 50 half-waves



- 33 half-waves



- 25 half-waves



With multichannel operation, the different channels should be operated with delayed half-waves in order to ensure that the load is placed evenly on the module.

Data type	Values
UINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Channel 1	0000	100 half-waves/second
		0001	50 half-waves/second
		0010	25 half-waves/second
		0011	33 half-waves/second
		0101	50 half-waves/second delayed by 1 half-wave
		0110	25 half-waves/second delayed by 2 half-waves
		0111	33 half-waves/second delayed by 1 half-wave
4 - 7	Channel 2	0000 to 0111	See channel 1.
8 - 11	Channel 3	0000 to 0111	See channel 1.
12 - 15	Channel 4	0000 to 0111	See channel 1

Information:

This function is available beginning with firmware version 940. This can be included beginning with hardware variant 8.

10.8.2 Setting the switch-off time

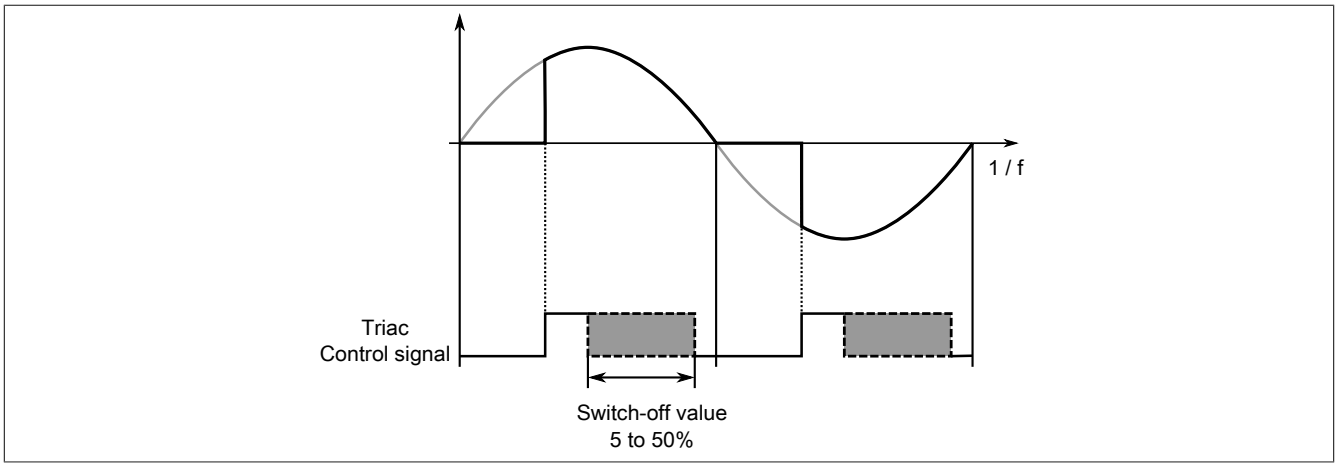
Name:
ConfigOutput01 to ConfigOutput04

This register defines how far in front of the zero cross-over the internal control signal for the TRIAC is switched off. Increasing this value may be necessary in order to prevent unwanted firing of the TRIAC in the event of a slight disturbance in the mains frequency.

With smaller loads, it is important to ensure that this switch off value is not set to large (too early) to prevent switching off prematurely.

The triac can of course only be fired before the set switch-off time.

"SwitchOffValue" in the Automation Studio I/O configuration.



Data type	Value	Description
USINT	5 to 50	Switch-off time in %. Bus controller default setting: 0

10.8.3 Configuration of the output channels

Name:
ConfigOutput05

The configuration of the output channels is stored in this register.

"Output type digital/analog" and "Output type full/half wave" in the Automation Studio I/O configuration

Data type	Values	Bus controller default setting
USINT	See the bit structure.	15

Bit structure:

Bit	Description	Value	Information
0	Channel 1: Digital/Analog output	0	Output channel 1 is defined as a digital output. The output status is defined by bit 0 of register "DigitalOutput 1 - 4" on page 8.
		1	Output channel 1 is defined as an analog output. The output status is defined by register "AnalogOutput01" on page 8 (bus controller default setting).
...		...	
3	Channel 4: Digital/Analog output	0	Output channel 4 is defined as a digital output. The output status is defined by bit 1 of register "DigitalOutput 1 - 4 " on page 8.
		1	Output channel 2 is defined as an analog output. The output status is defined by register "AnalogOutput04" on page 8 (bus controller default setting).
4	Channel 1: Full-wave/Half-wave control[1)]	0	Full-wave control on output channel 1 (bus controller default setting)
		1	Negative half-wave on output channel 1 is suppressed.
...		...	
7	Channel 4: Full-wave/Half-wave control[1)]	0	Full-wave control on output channel 4 (bus controller default setting)
		1	Negative half-wave on output channel 4 is suppressed.

1) Not available in function model 2 - Frequency mode.

10.8.4 Switching behavior for zero-crossing errors

Name:
CfO_OutputTolerance

This register can be used to set the switching behavior of the trigger. After the number of zero-crossing errors configured in Bit 0 to 4, the output is switched off for at least 3 periods. This is followed by synchronization with the zero signal according to Bit 7.

Data type	Values	Bus controller default setting
USINT	See bit structure.	0

Bit structure:

Bit	Description	Value	Information
0 - 4	Trigger for Resync	0 to 30	Number of zero crossing errors. Bus controller default setting: 0
5 - 6	Reserved	-	
7	Fast settling	0	Quick adjustment (bus controller default setting)
		1	PLL synchronization

Fast synchronization

With this option, the trigger point is closed-loop controlled after each individual zero-crossover and input jitter.

- **Advantage:** Increased tolerance and faster response to deviations in mains frequency
- **Disadvantage:** Increased switch-on jitter for firing signal by zero cross signal ±100 µSec

PLL synchronization

With this option the intervals between zero cross-overs are measured and the PLL frequency is updated accordingly.

- **Advantage:** Jitter-free firing signal
- **Disadvantage:** When the output is switched off, additional measurement phases are required before it can be switched back on.

Information:

This function is available starting with Firmware version 928. This can be installed with hardware version 7 and hardware revision B4 or higher.

10.9 Status of the outputs

Name:
ZeroCrossingInput
ZeroCrossingStatus
StatusInput01

The operating status of the outputs is mapped in this register.

Only function model 0 - Standard:

Setting "Packed outputs" in the Automation Studio I/O configuration determines whether all bits of this register should be applied individually as data points in the Automation Studio I/O assignment ("ZeroCrossingInput" to "ZeroCrossingStatus") or whether this register should be displayed as a single USINT data point ("StatusInput01").

Data type	Value	Information
USINT	0 to 255	Packed outputs = On
	See the bit structure.	Packed outputs = Off or function model ≠ 0 - Standard.

Bit structure:

Bit	Name	Value	Information
0 - 3	Reserved	-	
4	ZeroCrossingInput	0	Zero cross signal during the negative half-wave
		1	Zero cross signal during the positive half-wave
5 - 6	Reserved	-	
7	ZeroCrossingStatus	0	Zero cross signal OK
		1	Zero cross signal has dropped out

10.10 Function model "OSP"

In function model "OSP" (Operator Set Predefined), the user defines an analog value or digital pattern. This OSP value is output as soon as the communication between the module and master is aborted.

Functionality

The user has the choice between 2 OSP modes:

- Retain last valid value
- Replace with static value

In the first case, the module retains the last value recognized as a valid output status.

When selecting mode "Replace with static value", a plausible output value must be entered in the associated value register. When an OSP event occurs, this value is output instead of the value currently requested by the task.

10.10.1 Enabling OPS output in the module

Name:
OSPValid

This data point makes it possible to start the output of the module and request the use of OSP during operation.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	OSPValid	0	Request OSP operation (after initial startup or module in stand-by)
		1	Request normal operation
1 - 7	Reserved	0	

Bit OSPValid exists once on the module and is managed by the user task. It must be set to start the enabled channels. As long as bit OSPValid remains set in the module, the module behaves the same as in function model "Standard".

If an OSP event occurs, e.g. communication between the module and master CPU aborted, then bit OSPValid is reset on the module. The module enters the OSP state and output occurs according to the configuration in register "OSPMode" on page 13.

The following generally applies:

Even after regeneration of the communication channel, the OSP replacement value is still pending. The OSP state is only exited again when a set OSPValid bit is transferred.

When the master CPU is restarted, bit OSPValid bit is reinitialized in the master CPU. It must be set once more by the application and transferred via the bus.
In the event of brief communication errors between the module and master CPU(e.g. due to EMC), the cyclic registers fail to refresh for several bus cycles. Within the module, bit OSPValid is reset; the set bit is retained in the CPU, however. During the next successful transfer, the module-internal OSPValid bit is set again and the module automatically returns to normal operation.

If the task in the master CPU needs the information about which output mode the module is currently in, bit ModulOK can be evaluated.

Warning!

If bit OSPValid bit is reset to "0" by the module, the output status no longer depends on the responsible task in the master CPU. Nevertheless, output is made depending on the configuration of the OSP replacement value.

10.10.2 Setting OSP mode

Name:
CfgOSPMode

This register controls the behavior of a channel when using OSP.

Data type	Values	Explanation
USINT	0	Replace with static value
	1	Retain last valid value

10.10.3 Defining an OSP-digital output value

Name:
CfgOSPValue

This register contains the digital output value that is output in "Replace with static value" mode during OSP operation.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0		0 or 1	OSP output value for channel DigitalOutput00
...		...	
x		0 or 1	OSP output value for channel DigitalOutput0x

Warning!

"OSPValue" is only applied by the module if bit "OSPValid" has been set in the module.

10.10.4 Define the OSP analog output value

Name:
CfgOSPValue01 to CfgOSPValue04

This register contains the analog output value, which is output in "Replace with static value" mode during OSP operation.

Data type	Value
USINT	0 to 100

Warning!

"OSPValue" is only applied by the module if bit "OSPValid" has been set in the module.

10.11 Minimum cycle time

The minimum cycle time specifies the time up to which the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

	Minimum cycle time
All channels	250 µs

10.12 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

	Minimum I/O update time
All channels	150 µs