X20DC1178

1 General information

This module is equipped with one input for SSI absolute encoders with 5 V encoder signal. The data signal is monitored (Data, Data\).

- 1 SSI absolute encoder 5 V
- Monitoring the data signal
- 2 additional inputs
- 5 VDC, 24 VDC and GND for encoder supply
- NetTime timestamp: Counter change
- Can be used with a SafeLOGIC controller

NetTime timestamp of the counter

For many applications, not only the counter value is important, but also the exact time of the counter change. For this purpose, the module has a NetTime function that provides the recorded counter value with a timestamp accurate to microseconds.

The module provides the PLC with the counter value and timestamp as an absolute time value. The NetTime mechanisms ensure that the PLC NetTime clock and the local NetTime clock on the module have the same absolute time at all times.

2 Order data

Model number	Short description	Figure
	Counter functions	
X20DC1178	X20 digital counter module, 1 SSI absolute encoder, 5 V, 1 Mbit/s, 32-bit, encoder monitoring, NetTime function	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 1: X20DC1178 - Order data

3 Technical data

Model number	X20DC1178
Short description	
I/O module	1 SSI absolute encoder 5 V
General information	
B&R ID code	0xA708
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using LED status indicator and software
Power consumption	
Bus	0.01 W
Internal I/O	1.1 W
Additional power dissipation caused by actuators (resistive) [W]	-
Type of signal lines	Shielded cables must be used for all signal lines.
Certifications	
CE	Yes
KC	Yes
EAC	Yes
UL	cULus E115267 Industrial control equipment
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X
DNV GL	Temperature: **B** (0 - 55°C) Humidity: **B** (up to 100%) Vibration: **B** (4 g) EMC: **B** (bridge and open deck)
LR	ENV1
Digital inputs	
Quantity	2
Nominal voltage	24 VDC
Input characteristics per EN 61131-2	Type 1
Input voltage	24 VDC -15% / +20%
Input current at 24 VDC	Approx. 3.3 mA
Input circuit	Sink
Input filter	
Hardware	≤2 µs
Software	-
Connection type	3-wire connections
Input resistance	7.03 kΩ
Switching threshold	
Low	<5 VDC
High	>15 VDC
Isolation voltage between channel and bus	500 V_{eff}
SSI absolute encoder	
Encoder inputs	5 V, symmetrical
Counter size	Up to 32-bit depending on encoder
Max. transfer rate	1 Mbit/s
Keying	Gray/Binary
Minimum diff. slew rate	1 V/µs
Isolation voltage between encoder and bus	500 V_{eff}
Overload characteristics of encoder power supply	Short-circuit proof, overload-proof
Transfer rate	125 kbit/s / 250 kbit/s / 500 kbit/s / 1 Mbit/s
Encoder power supply	
5 VDC	±5%, module-internal, max. 300 mA
24 VDC	Module-internal, max. 300 mA
Switching threshold	
Low	>1 V
Electrical properties	
Electrical isolation	Channel isolated from bus Channel not isolated from channel
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation elevation above sea level	
0 to 2000 m	No limitation
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m

Table 2: X20DC1178 - Technical data

Model number	X20DC1178
Degree of protection per EN 60529	IP20
Ambient conditions	
Temperature	
Operation	
Horizontal mounting orientation	-25 to 60°C
Vertical mounting orientation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical properties	
Note	Order 1x terminal block X20TB12 separately. Order 1x bus module X20BM11 separately.
Spacing	12.5 $^{+0.2}$ mm

Table 2: X20DC1178 - Technical data

4 LED status indicators

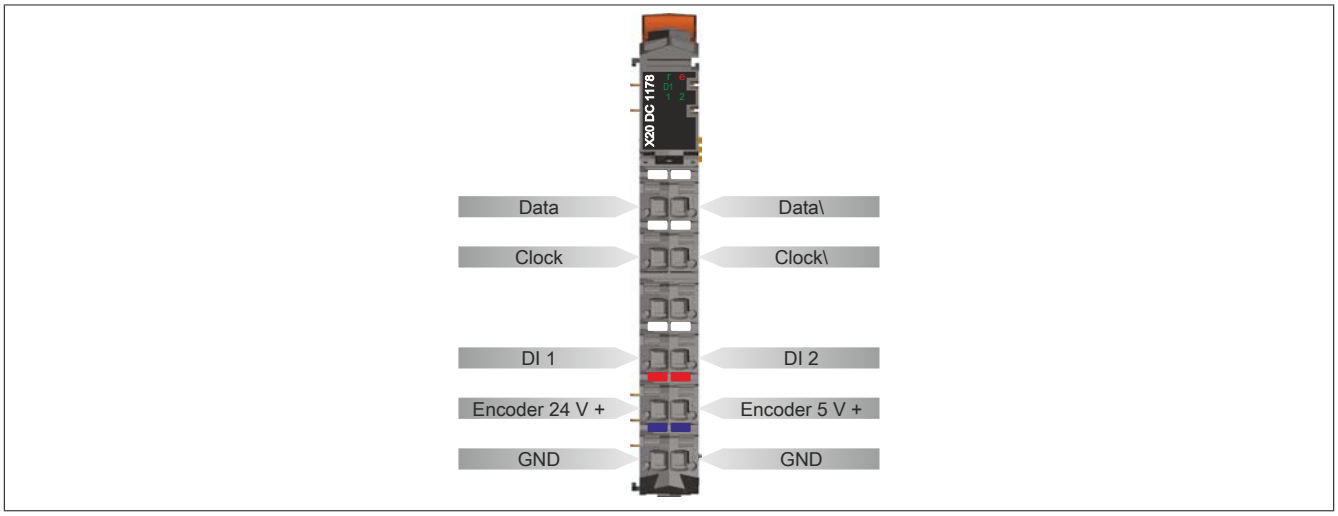
For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" of the X20 system user's manual.

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1)]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			Single flash	Either the encoder monitor has detected a line fault on the encoder inputs or a transfer error has occurred. The status bits must be evaluated in order to provide a more detailed definition of this error. The following error states are detected: • Open line • Short-circuit or voltage level too low • SSI cycle time violation • Parity error
			On	Error or reset status
	D1	Green		Input status - Data signal
	1 - 2	Green		Input state of the corresponding digital input

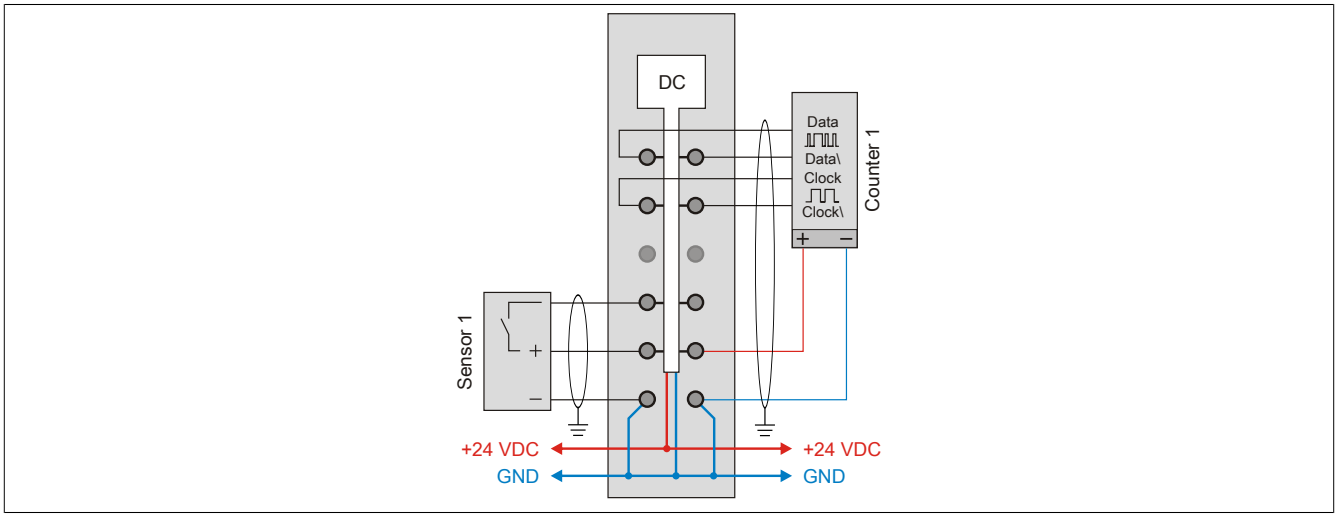
1) Depending on the configuration, a firmware update can take up to several minutes.

5 Pinout

Shielded cables must be used for all signal lines.

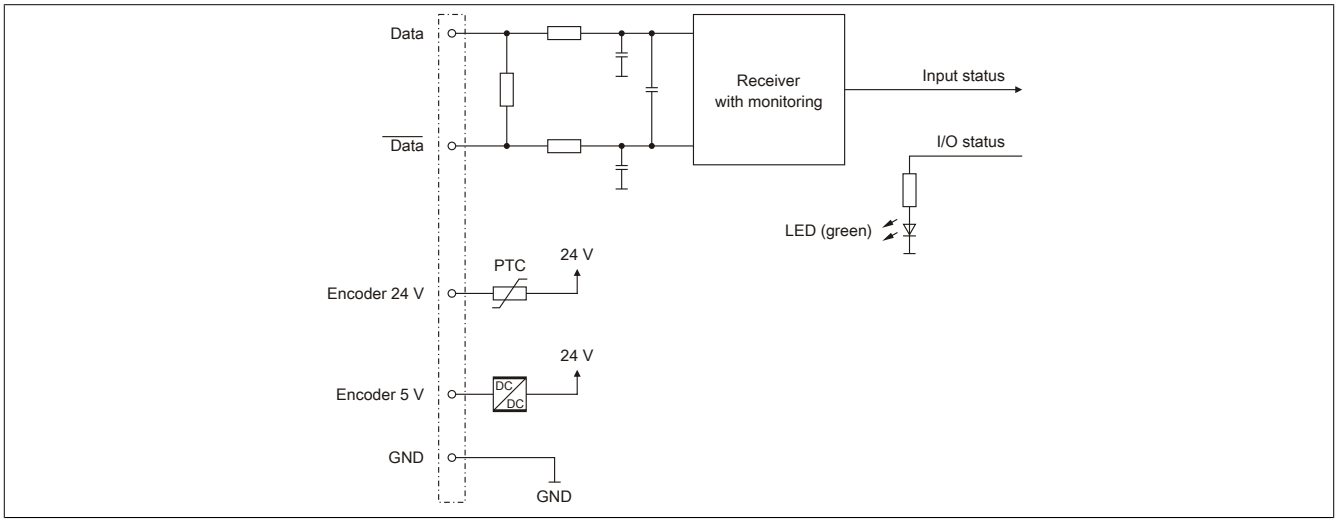


6 Connection example

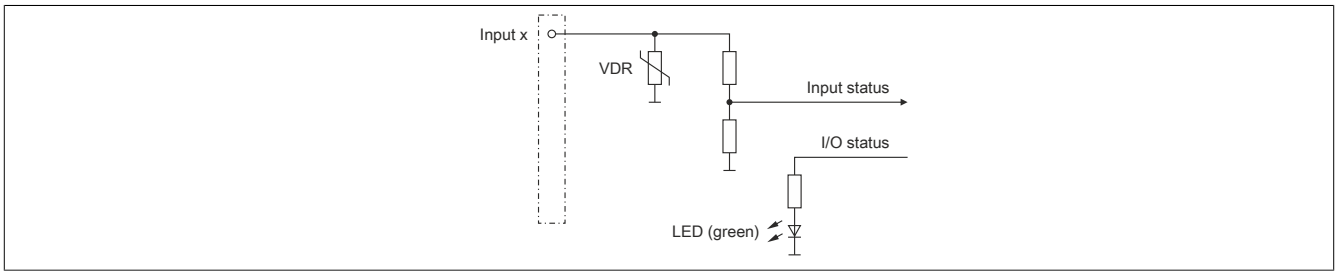


7 Input circuit diagram

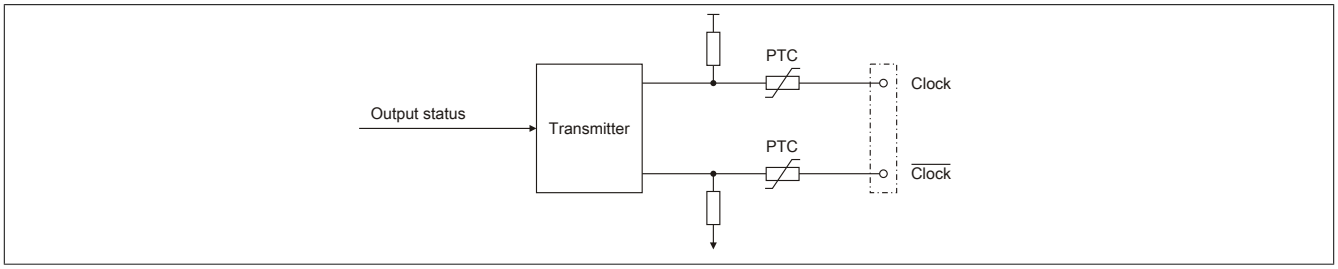
Counter input



Standard inputs



8 Output circuit diagram



9 Register description

9.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" of the X20 system user's manual.

9.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration						
650	CfO_SystemCyclePrescaler	UINT				•
2049	CfO_CycleSelect	USINT				•
2951	CfO_PhysicalMode	USINT				•
2053	CfO_DataBits	USINT				•
2055	CfO_NullBits	USINT				•
820	CfO_BWQuitTime_0	UDINT				•
815	CfO_BWQuitTimeSelChannel7_0	USINT				•
2059	CfO_BWSSIEnableMaskChannel7_0	USINT				•
Communication						
683	SDCLifeCount	SINT	•			
927	Input status of signal lines	USINT	•			
	DigitalInput01	Bit 4				
	DigitalInput02	Bit 5				
2100	Encoder01	(U)DINT	•			
2102	Encoder01	UINT	•			
2086	Encoder01TimeValid	INT	•			
2084	Encoder01TimeValid	DINT	•			
2094	Encoder01TimeChanged	INT	•			
2092	Encoder01TimeChanged	DINT	•			
259	State of the encoder	USINT	•			
	EncoderCycleTimeViolation	Bit 0				
	EncoderDataError	Bit 1				
323	Acknowledging error status of the encoder	USINT			•	
	EncoderQuitCycleTimeViolation	Bit 0				
	EncoderQuitDataError	Bit 1				
847	Status of signal lines	USINT	•			
	BW_Channel_D	Bit 0				
811	Acknowledging error status of the signal line	USINT			•	
	BW_QuitChannel_D	Bit 0				
843	Status of encoder supplies	USINT	•			
	PowerSupply01	Bit 0				
	PowerSupply02	Bit 1				

SafeLOGIC registers

This module contains additional registers that allow the module to be used with a SafeLOGIC controller.

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration						
7234	CfO_DTS_SourceRef	INT				•
7237	CfO_DTS_CycleSelect	USINT				•
Communication						
7252	Encoder01	DINT	•			
7260	Encoder01TimeValid	DINT	•			
7266	DTS_SourceRef	INT	•			
7270	DTS_CheckSum	INT	•			

9.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration							
650	-	CfO_SystemCyclePrescaler	UINT				•
2049	-	CfO_CycleSelect	USINT				•
2051	-	CfO_PhysicalMode	USINT				•
2053	-	CfO_DataBits	USINT				•
2055	-	CfO_NullBits	USINT				•
820	-	CfO_BWQuitTime_0	UDINT				•
815	-	CfO_BWQuitTimeSelChannel7_0	USINT				•
2059	-	CfO_BWSSIEnableMaskChannel7_0	USINT				•
Communication							
683		SDCLifeCount	SINT	•			
927	7	Input status of signal lines	USINT	•			
		DigitalInput01	Bit 4				
		DigitalInput02	Bit 5				
2100	-	Encoder01	(U)DINT	•			
2086	4	Encoder01TimeValid	INT	•			
2094	-	Encoder01TimeChanged	INT	•			
259	-	State of the encoder	USINT	•			
		EncoderCycleTimeViolation	Bit 0				
		EncoderDataError	Bit 1				
323	-	Acknowledging error status of the encoder	USINT			•	
		EncoderQuitCycleTimeViolation	Bit 0				
		EncoderQuitDataError	Bit 1				
847	6	Status of signal lines	USINT	•			
		BW_Channel_D	Bit 0				
811	0	Acknowledging error status of the signal line	USINT			•	
		BW_QuitChannel_D	Bit 0				
843	-	Status of encoder supplies	USINT	•			
		PowerSupply01	Bit 0				
		PowerSupply02	Bit 1				

1) The offset specifies the position of the register within the CAN object.

9.3.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use additional registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" of the X20 user's manual (version 3.50 or later).

9.3.2 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN I/O.

9.4 Encoder - Configuration

The following registers are used for setting functions and configuring the module.

9.4.1 Setting the SSI sampling cycle time

The following two registers define the cycle time for SSI sampling.

9.4.1.1 Setting the interrupt

Name:

CfO_CycleSelect

This register assigns the principle interrupt setting:

- **Timer configuration (time setting with "CfO_SystemCyclePrescaler" on page 8 register):** The SSI transfer can be started independently of the X2X cycle. The timer is synchronized with X2X Link.
- **AOAI:** Configuration with X2X interrupt, one-time start of the SSI transfer in the X2X cycle. The SSI transfer may require an entire X2X cycle.
- **SOSI:** Configuration with X2X interrupt, one-time start of the SSI transfer in the X2X cycle. The reaction time can be optimized with this setting if the SSI transfer doesn't exceed half of an X2X cycle.

Data type	Value	Filter
USINT	3	Timer [µsec] ... Time setting with register "CfO_SystemCyclePrescaler" on page 8
	10	AOAI (bus controller default setting)
	14	SOSI

9.4.1.2 Setting the cycle time

Name:

CfO_SystemCyclePrescaler

The desired cycle time must be configured additionally for the timer setting using this register.

Data type	Value	Filter
USINT	1	50 µs
	2	100 µsec (bus controller default setting)
	4	200 µs
	8	400 µs
	16	800 µs
	0	All other settings in the "CfO_CycleSelect" on page 8 register

9.4.2 Setting operating parameters

Name:
CfO_PhysicalMode

This register defines the operating parameters for the SSI encoder to correctly evaluate the data from the encoder.

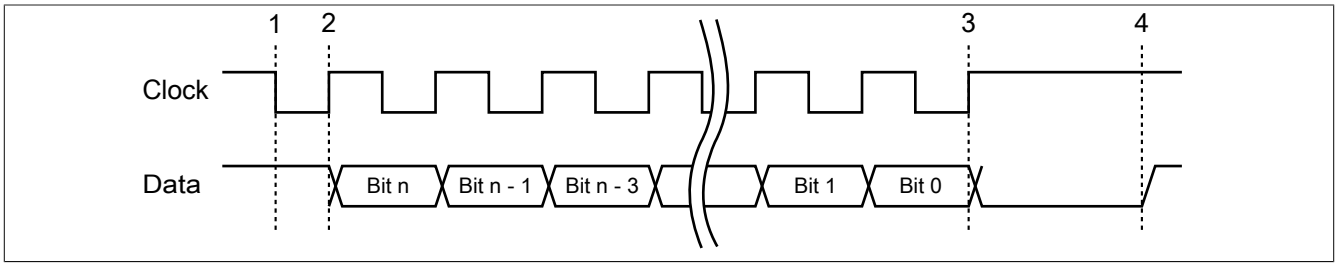
- **Parity:** Data with or without parity; an error is reported if there is an even or uneven parity mismatch.
- **Monoflop check:** The encoder uses the monoflop to signal the readiness to accept a new clock cycle.
- **Data coding:** Binary or gray coding of the data bits
- **Clock rate:** Speed of data transfer

Data type	Values	Bus controller default setting
USINT	See the bit structure.	0

Bit structure:

Bit	Name	Value	Information
0 - 1	Parity bit	00	No parity bit (no clock bit output) (bus controller default setting)
		01	Even parity bit
		10	Uneven parity bit
		11	Ignore parity bit (clock bit is output, but the result is ignored)
2 - 3	Monostable multivibrator testing	00	No monostable multivibrator check (no clock bit output) (bus controller default setting)
		01	Check - Low level
		10	Check - High level
		11	Check - Ignore level (clock bit is output, but the result is ignored)
4	Data coding	0	Binary coding (bus controller default setting)
		1	Gray coding
5	Reserved	0	
6 - 7	Clock rate	00	1 MHz (bus controller default setting)
		01	500 kHz
		10	250 kHz
		11	125 kHz

Transfer to synchronous serial interface



Measurement value processing

1) Starting bit ... Stores the measurement value
2) Output of first data bit
3) All data bits are transferred, monostable multivibrator time starts counting down.
4) Monostable multivibrator returns to its initial state. A new transfer can be started.

9.4.3 Number of data bits

Name:

Cfo_DataBits

This register can be used to define the number of SSI encoder data bits.

Data type	Value	Filter
USINT	1 to 32	Number of SSI data bits; Bus controller default setting: 0

9.4.4 Leading zeros of the encoder

Name:

Cfo_NullBits

This register can be used to define the number of SSI encoder leading zeros.

Data type	Value	Filter
USINT	1 to 32	Number of leading zeros; Bus controller default setting: 0

9.4.5 Timing for automatic error acknowledgment

Name:
CfO_BWQuitTime_0

This register can be used to enable an additional automatic acknowledgment of the error status through timing. If a valid time is set, then the acknowledgment can still be made manually, the only difference is that automatic acknowledgment will take place on the module after the defined amount of time has passed. If the error state has not yet been corrected, then the error status remains and the time is reset. Make sure that the time is set long enough for the higher-level system to reliably detect the status messages.
If the timing = 0, then acknowledgment is only possible using the cyclic acknowledgment registers.

Data type	Value	Information
UDINT	0	No automatic acknowledgment. Bus controller default setting
	1 to 2.147.483.647	Time for automatic acknowledgment [µs]

9.4.5.1 Automatic acknowledgment of latched error states

In addition to manual acknowledgment, automatic acknowledgment of the latched error states after a specified amount of time can also be enabled. Make sure that the time is set long enough for the higher-level system to reliably detect the status messages and for the validity of the counter value to be determined using its age.

If the time specification = 0, then only manual acknowledgment is possible.

Example 1: An error has occurred on a signal line. The error state is detected and latched by the module. The time for automatic acknowledgment starts counting after the cause of error has been corrected. The error is acknowledged as soon as the time expires. The latched error status changes to zero.

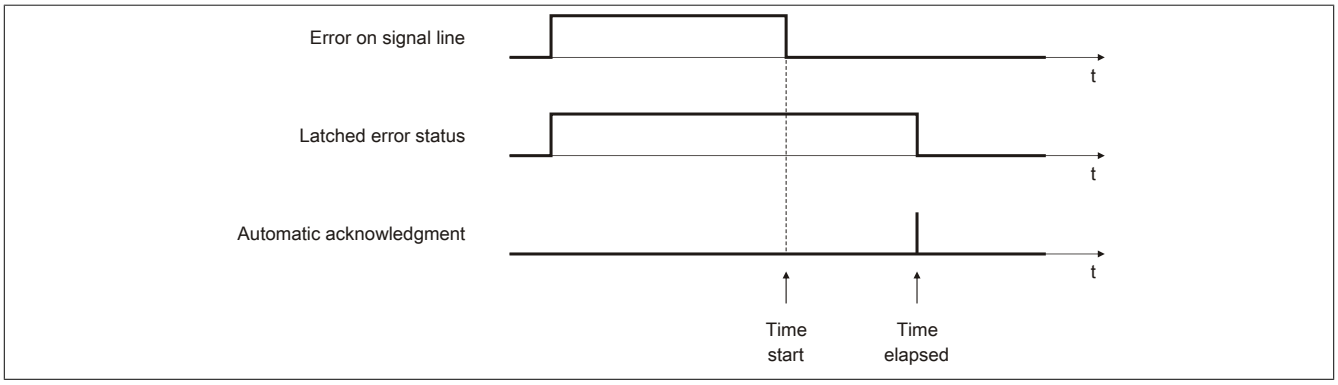


Figure 1: Latched error state acknowledged automatically

Example 2: Automatic and manual acknowledge used

An error has occurred on a signal line. The error state is detected and latched by the module. The time for automatic acknowledgment starts counting after the cause of error has been corrected. The error is acknowledged manually by the user before the time expires. The latched error status changes to zero. The manual acknowledge must now be reset so that any new errors will be recognized by the user.

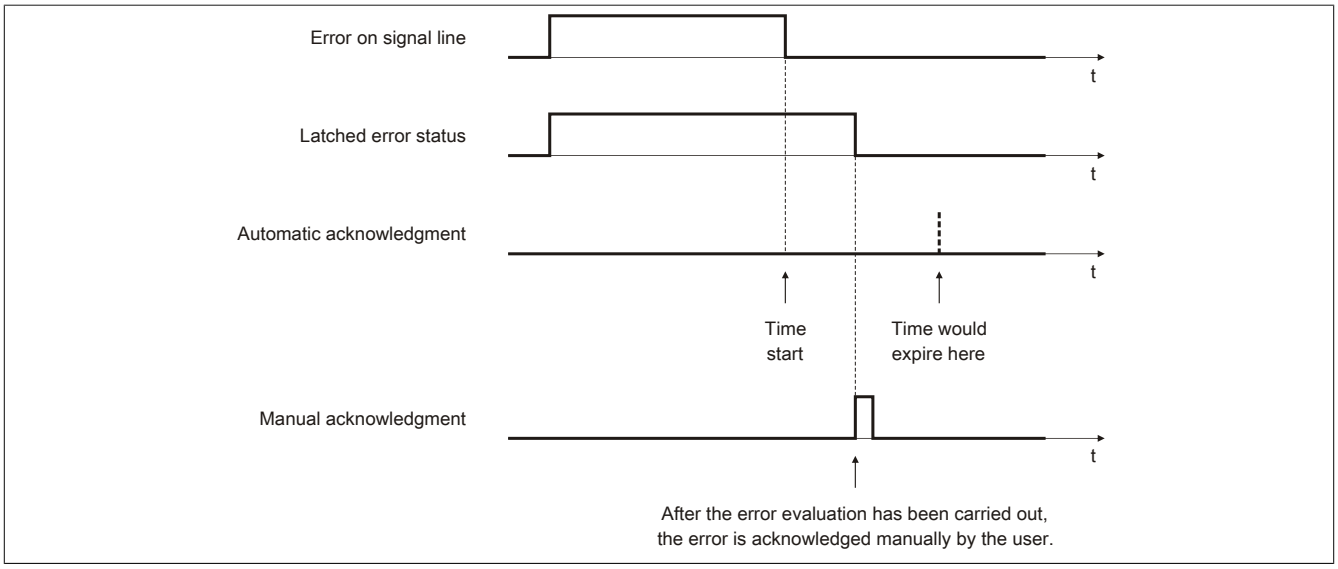


Figure 2: Automatic and manual acknowledge used

9.4.5.2 Manual acknowledgment of latched error states

The latched error states of the signal lines from the encoder can be acknowledged manually. However, if there are still pending errors remaining, then the error status remains active. After successfully acknowledging the errors (latched error status = 0), the acknowledge bits must still be reset by the user or else a re-occurrence of an error could be overlooked by the user.

Example 1: **Cause of error corrected before being acknowledged**

An error has occurred on a signal line. The error state is detected and latched by the module. The error is acknowledged by the user after the cause of error has been corrected. The latched error status changes to zero.
The manual acknowledge must now be reset so that any new errors will be recognized by the user.

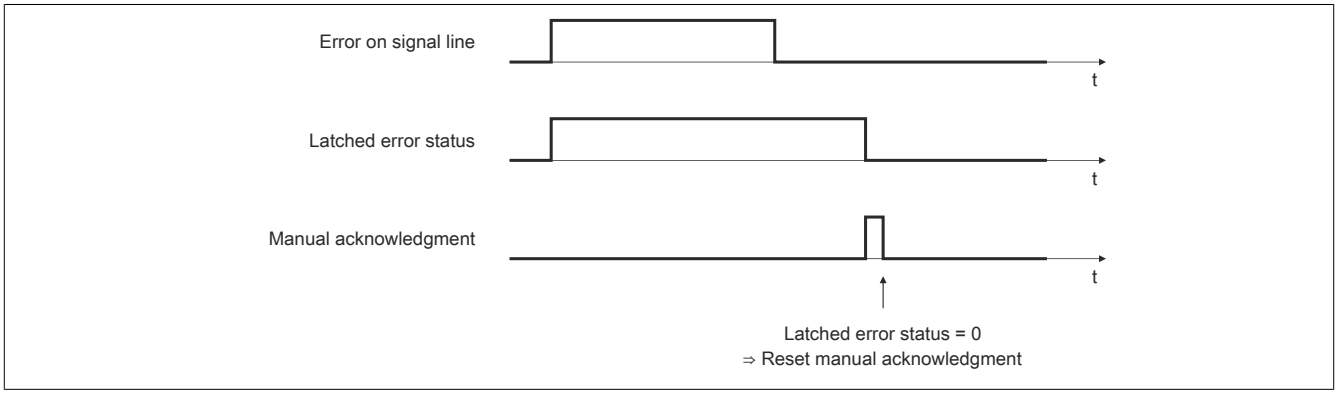


Figure 3: Cause of error corrected before being acknowledged

Example 2: **Cause of error not yet corrected before being acknowledged**

An error has occurred on a signal line. The error state is detected and latched by the module. The error is acknowledged by the user before the cause of error has been corrected. The latched error status remains set because the error is still remaining.
Acknowledgment is only successful after the cause of error has been corrected. The latched error status changes to zero. The manual acknowledge must now be reset so that any new errors will be recognized by the user.

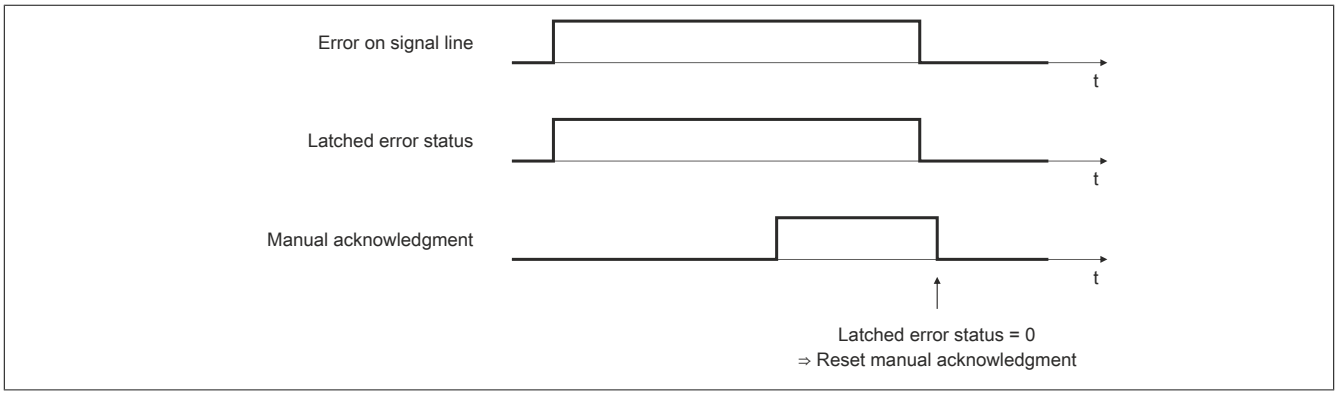


Figure 4: Cause of error not yet corrected before being acknowledged

9.4.6 Enable/disable error monitoring for the signal channels

Name:
CfO_BWSSIEnableMaskChannel7_0

This register allows error monitoring for each of the signal channels to be enabled individually. "Open line", "short circuit" and "voltage level too low" are reported as error states. Any errors that occur are reported in the error status registers.

Data type	Values	Bus controller default setting
USINT	See bit structure.	1

Bit structure:

Bit	Name	Value	Information
0	Encoder signal D	0	Error monitoring switched off
		1	Error monitoring enabled (bus controller default setting)
1 - 7	Reserved	0	

9.4.7 Physical configuration

The following registers must be set to the specified constant value for correct physical configuration:

9.4.7.1 Constant register "CfO_BWQuitTimeSelChannel7_0"

Name:
CfO_BWQuitTimeSelChannel7_0

Data type	Value	Information
USINT	0	Bus controller default setting

9.5 Encoder - Communication

9.5.1 Counter for verifying the data frame

Name:
SDCLifeCount

The 8-bit counter register is needed for the SDC software package. It is incremented with the system clock to allow the SDC to check the validity of the data frame.

Data type	Value
SINT	-128 to 127

9.5.2 Input status of signal lines

Name:
DigitalInput0 to DigitalInput02

This register displays the input states for the digital inputs.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 3	Reserved	0	
4	DigitalInput01	0 or 1	Input state - Digital input 1
5	DigitalInput02	0 or 1	Input state - Digital input 2
6 - 7	Reserved	0	

9.5.3 Display of the counter state

Name:
Encoder01

The counter state of the incremental encoder is displayed as a 16 or 32-bit counter value.

Data type	Value
UDINT	0 to 4.294.967.295
DINT	-2.147.483.648 to 2.147.483.647
UINT[1)]	0 to 65535

1) Only available in function model 0

9.5.4 NetTime of the last valid counter value

Name:
Encoder01TimeValid

The NetTime of the last valid counter value is the time of the last valid counter value recorded on the module. The user is able to determine the validity of the counter value by evaluating its age in the program. This means that the module and error status bits do not have to be checked additionally to determine the validity of the value.

The NetTime of the last valid counter value that was read is displayed as a 16 or 32-bit value. Only the 16-bit value is available in the bus controller function model.

For more information about NetTime and timestamps, see "NetTime technology" on page 19.

Data type	Value	Information
INT	-32768 to 32767	NetTime in µs
DINT[1)]	-2.147.483.648 to 2.147.483.647	

1) Can only be configured in the standard function model

9.5.5 NetTime of the last counter value change

Name:
Encoder01TimeChanged

For slow X2X Link cycles, the NetTime of the last counter value change can be used to determine the speed more accurately.

The NetTime of the last counter value change is displayed as a 16 or 32-bit value. Only the 16-bit value is available in the bus controller function model.

For more information about NetTime and timestamps, see "NetTime technology" on page 19.

Data type	Value	Information
INT	-32768 to 32767	NetTime in µs
DINT[1)]	-2.147.483.648 to 2.147.483.647	

1) Can only be configured in the standard function model

9.5.6 State of the encoder

Name:
EncoderCycleTimeViolation
EncoderDataError

This register displays the error states that occurred while determining the position. The error states are latched when they occur and are maintained until acknowledged.

A cycle time error is triggered if:

- Transfer is still active: This means that the defined cycle time is shorter than the time resulting from the sum of the data bits and stop bits and the clock rate.
- The monoflop level does not match the defined start level
- There is an error pending on the signal line (open line, short circuit).

A data error is triggered if:

- The parity bit does not match.
- An error occurs on the signal line (open line, short circuit) during transfer.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	EncoderCycleTimeViolation	0	No error
		1	Error status - Cycle time violation
1	EncoderDataError	0	No error
		1	Error status - Data error
2 - 7	Reserved	0	

9.5.7 Acknowledging error status of the encoder

Name:
EncoderQuitCycleTimeViolation
EncoderQuitDataError

This register can be used to acknowledge the latched data error states from the encoder. However, if there are still pending errors remaining, then the error status remains active. After acknowledging the errors, the bits must also be reset or else any repetition of the error would be undetected.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	EncoderQuitCycleTimeViolation	0	No acknowledgment
		1	Confirmation of error status - Cycle time violation
1	EncoderQuitDataError	0	No acknowledgment
		1	Confirmation of error status - Data error
2 - 7	Reserved	0	

9.5.8 Status of signal lines

Name:
BW_Channel_D

This register displays the error state of the signal line from the encoder. The error state is latched when it occurs and is maintained until acknowledged. The counter and time registers are not updated if there are pending or unacknowledged errors.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	BW_Channel_D	0	No error - Encoder signal D
		1	Error status - Open line or short circuit (voltage level too low)
1 - 7	Reserved	0	

9.5.9 Acknowledging error status of the signal line

Name:
BW_QuitChannel_D

This register can be used to acknowledge the latched error states of the signal lines from the encoder. However, if there are still pending errors remaining, then the error status remains active. After acknowledging the errors, the bit must also be reset or else any repetition of the error will be undetected.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	BW_QuitChannel_D	0	No acknowledgment
		1	Acknowledgment of error status
1 - 7	Reserved	0	

9.5.10 Status of encoder supplies

Name:
PowerSupply01 to PowerSupply02

This register shows the status of the integrated encoder supplies. A faulty encoder power supply is displayed as a warning.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	PowerSupply01	0	24 VDC encoder power supply OK
		1	24 VDC encoder power supply faulty
1	PowerSupply02	0	5 VDC encoder power supply OK
		1	5 VDC encoder power supply faulty
2 - 7	Reserved	-	

9.6 DATA_to_SafeDATA

Function DATA_to_SafeDATA determines a safe signal from 2 independent standard signals. For this purpose, the standard data of 2 I/O modules are transferred to the SafeLOGIC controller and compared with each other there. With the functions provided in SafeDESIGNER, the resulting data can be used for applications up to PL d.

Function DATA_to_SafeDATA is enabled and the register calls take place using SafeDESIGNER. For more detailed information on the calls, see library DATA_to_SafeDATA_SF contained in SafeDESIGNER.

9.6.1 Counter state of the encoder

Name:
Encoder01

This register represents the counter value of the encoder. The register is only active if function DATA_to_SafeDATA is enabled.

Data type	Values
DINT	-2,147,483,648 to 2,147,483,647

9.6.2 NetTime of the counter value

Name:
Encoder01TimeValid

This register represents the NetTime of the most recent valid counter value. The register is only active if function DATA_to_SafeDATA is enabled.

For a description of NetTime Technology, see "NetTime technology" on page 19.

Data type	Values
DINT	-2,147,483,648 to 2,147,483,647

9.6.3 Displaying the SourceRef address

Name:
DTS_SourceRef

This register cyclically displays the SourceRef address set in the configuration. The register is only active if function DATA_to_SafeDATA is enabled.

Data type	Values
INT	-32768 to 32767

9.6.4 Checksum

Name:
DTS_CheckSum

This register contains a checksum formed from the 3 cyclic data points Encoder01, Encoder01TimeValid and DTS_SourceRef. The register is only active if function DATA_to_SafeDATA is enabled.

Data type	Values
INT	-32768 to 32767

9.6.5 SourceRef address

Name:
CfO_DTS_SourceRef

This register contains the acyclically configurable SourceRef address that is sent back by the module as a cyclic data point. The register is only active if function DATA_to_SafeDATA is enabled.

Data type	Values
INT	-32768 to 32767

9.6.6 Constant cycle register

Name:
CfO_DTS_CycleSelect

This register determines the cycle used internally and is not permitted to be changed.

Data type	Value
USINT	2

9.7 NetTime technology

NetTime refers to the ability to precisely synchronize and transfer system times between individual components of the controller or network (CPU, I/O modules, X2X Link, POWERLINK, etc.).

This allows the time that events occur to be determined system-wide with microsecond precision. Upcoming events can also be executed precisely at a given time.

9.7.1 Time information

Various time information is available in the controller or on the network:

- System time (on the PLC, Automation PC, etc.)
- X2X Link time (for each X2X Link network)
- POWERLINK time (for each POWERLINK network)
- Time data points of I/O modules

The NetTime is based on 32-bit counters, which are increased with µs timing. The sign of the time information changes after 35 min, 47 s, 483 ms and 648 µs; an overflow occurs after 71 min, 34 s, 967 ms and 296 µs.

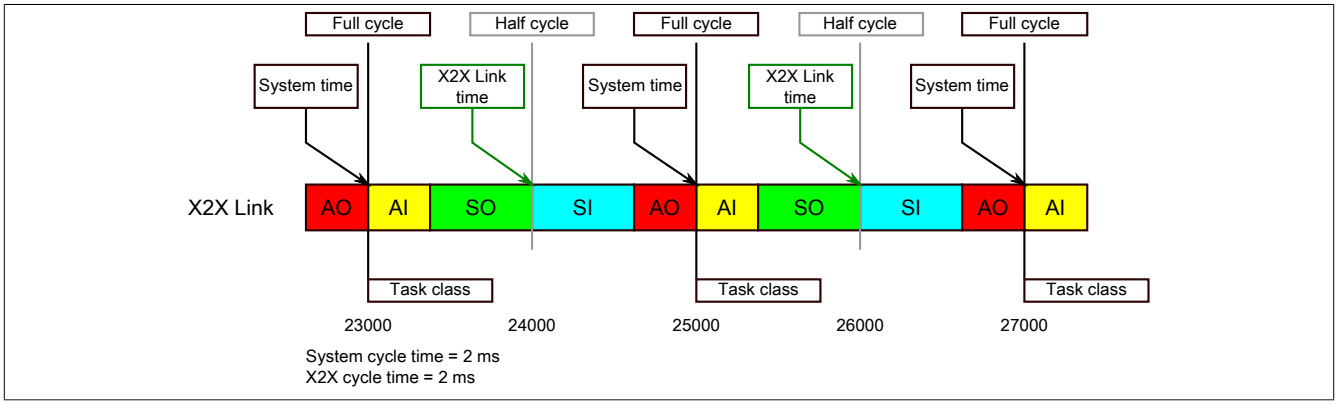
The initialization of the times is based on the system time during the startup of the X2X Link, the I/O modules or the POWERLINK interface.

Current time information in the application can also be determined via library AsIOTime.

9.7.1.1 PLC/Controller data points

The NetTime I/O data points of the PLC or the controller are latched to each system clock and made available.

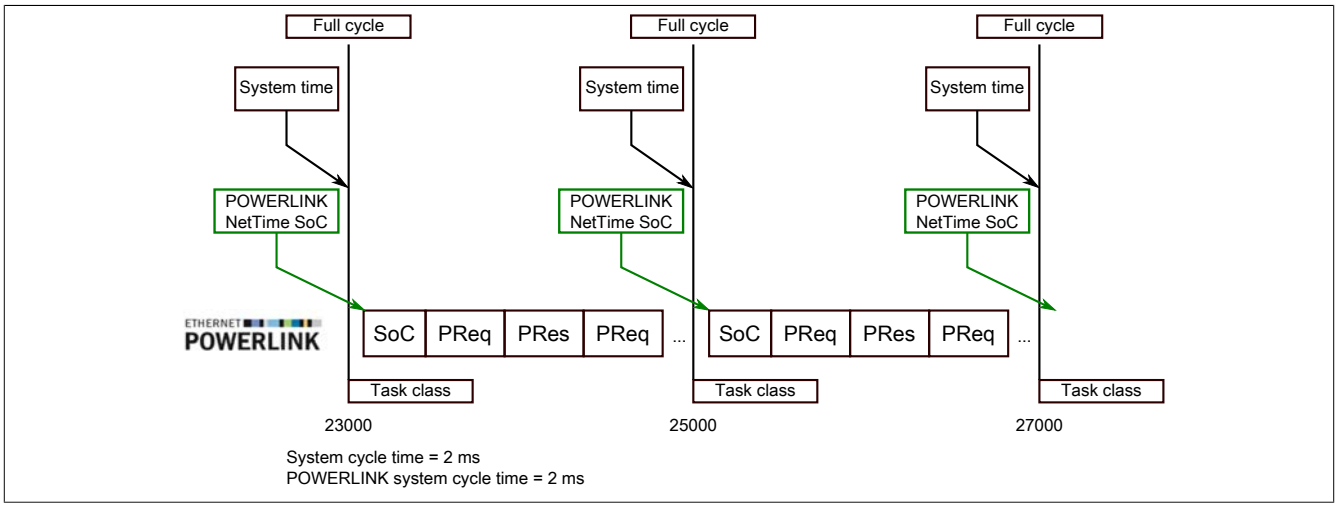
9.7.1.2 X2X Link reference time



The reference time on the X2X Link network is always formed at the half cycle of the X2X Link cycle. This results in a difference between the system time and the X2X Link reference time when the reference time is read out.

In the example above, this results in a difference of 1 ms, i.e. if the system time and X2X Link reference time are compared at time 25000 in the task, then the system time returns the value 25000 and the X2X Link reference time returns the value 24000.

9.7.1.3 POWERLINK reference time

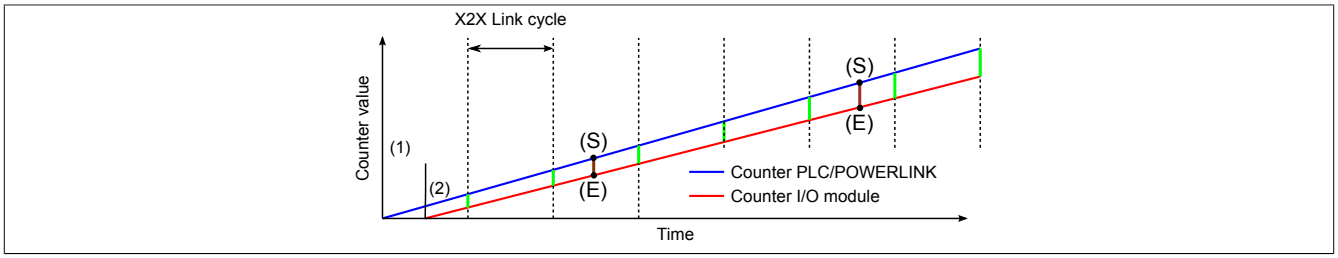


The reference time at POWERLINK is always formed at the SoC (Start of Cycle) of the POWERLINK network. The SoC starts 20 µs after the system tick. This results in the following difference between the system time and the POWERLINK reference time:

POWERLINK reference time = System time - POWERLINK cycle time + 20 µs.

In the example above, this means a difference of 1980 µs, i.e. if the system time and POWERLINK reference time are compared at time 25000 in the task, then the system time returns the value 25000 and the POWERLINK reference time returns the value 23020.

9.7.1.4 Synchronization of system time/POWERLINK time and I/O module



At startup, the internal counters for the PLC/POWERLINK (1) and the I/O module (2) start at different times and increase the values at µs intervals.

At the beginning of each X2X Link cycle, the PLC or the POWERLINK network sends time information to the I/O module. The I/O module compares this time information with the module's internal time and forms a difference (green line) between the two times and stores it.

When a NetTime event (E) occurs, the internal module time is read out and corrected with the stored difference value (brown line). This means that the exact system time (S) of an event can always be determined, even if the counters are not absolutely synchronous.

Note

The deviation from the clock signal is strongly exaggerated in the picture as a red line.

9.7.2 Timestamp functions

NetTime-capable modules provide various timestamp functions depending on the scope of functions. If a timestamp event occurs, the module immediately saves the current NetTime. After the respective data is transferred to the CPU, including this precise time, the CPU can then evaluate the data using its own NetTime (or system time), if necessary.

9.7.2.1 Time-based inputs

NetTime Technology can be used to determine the exact time of a rising edge at an input. The rising and falling edges can also be detected and the duration between 2 events can be determined.

> **Information:**
>
> **The determined time always lies in the past.**

9.7.2.2 Time-based outputs

NetTime Technology can be used to specify the exact time of a rising edge at an output. The rising and falling edges can also be specified and a pulse pattern generated from them.

> **Information:**
>
> **The specified time must always be in the future and the set X2X Link cycle time must be taken into account for the definition of the time.**

9.7.2.3 Time-based measurements

NetTime Technology can be used to determine the exact time of a measurement that has taken place. Both the start and the end time of the measurement can be transmitted.

9.8 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without causing a communication error or impaired functionality. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
150 µs

9.9 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
150 µs