X20DC2398

1 General information

This module is equipped with two inputs for SSI absolute encoders with 24 V encoder signal.

- 2 SSI absolute encoder 24 V
- 2 additional inputs
- 24 VDC and GND for encoder supply

2 Order data

Model number	Short description	Figure
	Counter functions	
X20DC2398	X20 digital counter module, 2 SSI absolute encoder, 24 V, 125 kbit/s, 32-bit	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 1: X20DC2398 - Order data

3 Technical data

Model number	X20DC2398
Short description	
I/O module	2 SSI absolute encoder 24 V
General information	
Input voltage	24 VDC -15 % / +20 %
B&R ID code	0x1BAD
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Power consumption	
Bus	0.01 W
Internal I/O	1.4 W
Additional power dissipation caused by actuators (resistive) [W]	-
Type of signal lines	Shielded cables must be used for all signal lines

Table 2: X20DC2398 - Technical data

Model number	X20DC2398
Certifications	
CE	Yes
KC	Yes
EAC	Yes
UL	cULus E115267 Industrial control equipment
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X
DNV GL	Temperature: **B** (0 - 55°C) Humidity: **B** (up to 100%) Vibration: **B** (4 g) EMC: **B** (bridge and open deck)
LR	ENV1
Digital inputs	
Quantity	2
Nominal voltage	24 VDC
Input current at 24 VDC	Approx. 3.3 mA
Input characteristics per EN 61131-2	Type 1
Input filter	
Hardware	≤2 µs
Software	-
Connection type	3-wire connections
Input circuit	Sink
Input resistance	7.19 kΩ
Switching threshold	
Low	<5 VDC
High	>15 VDC
Isolation voltage between channel and bus	500 V_{eff}
SSI absolute encoder	
Encoder inputs	24 V, asymmetrical
Counter size	32-bit
Max. transfer rate	125 kbit/s
Encoder power supply	Module-internal, max. 600 mA
Coding	Gray/Binary
CLK: Output current	Max. 100 mA
DATA: Input resistance	18.4 kΩ
Isolation voltage between encoder and bus	500 V_{eff}
Overload characteristics of encoder power supply	Short circuit protection, overload protection
Switching threshold	
Low	<5 VDC
High	>15 VDC
Electrical properties	
Electrical isolation	Bus isolated from encoder and channel Channel not isolated from channel and encoder Encoder not isolated from encoder
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation elevation above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
Degree of protection per EN 60529	IP20
Ambient conditions	
Temperature	
Operation	
Horizontal mounting orientation	-25 to 60°C
Vertical mounting orientation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical properties	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 2: X20DC2398 - Technical data

4 LED status indicators

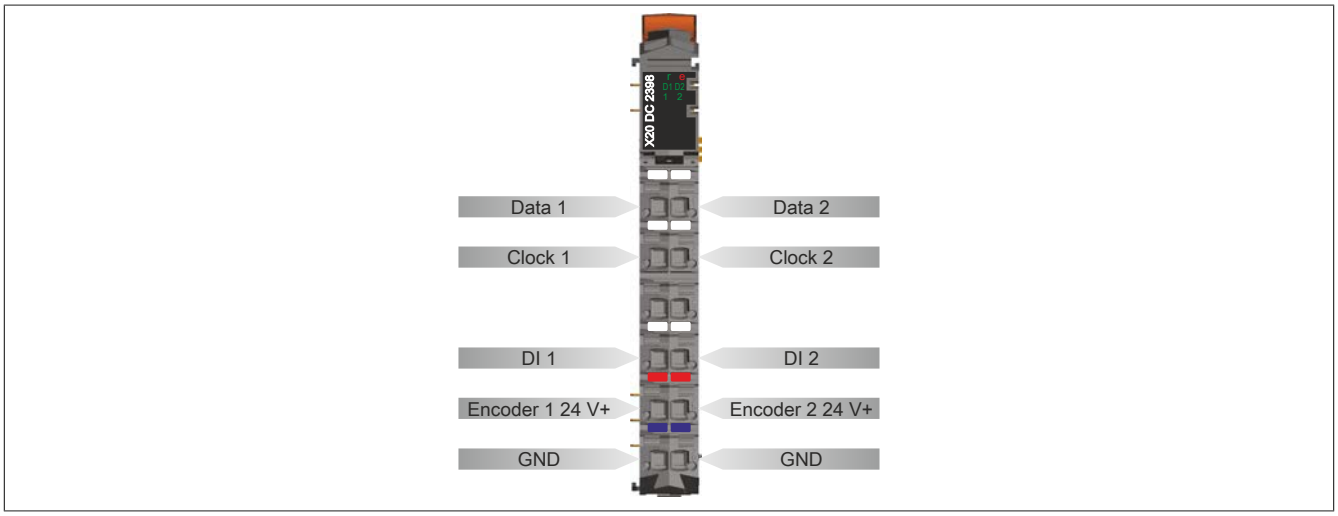
For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" of the X20 system user's manual.

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1)]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	D1, D2	Green		Input state of data signal 1 or 2
	1 - 2	Green		Input state of the corresponding digital input

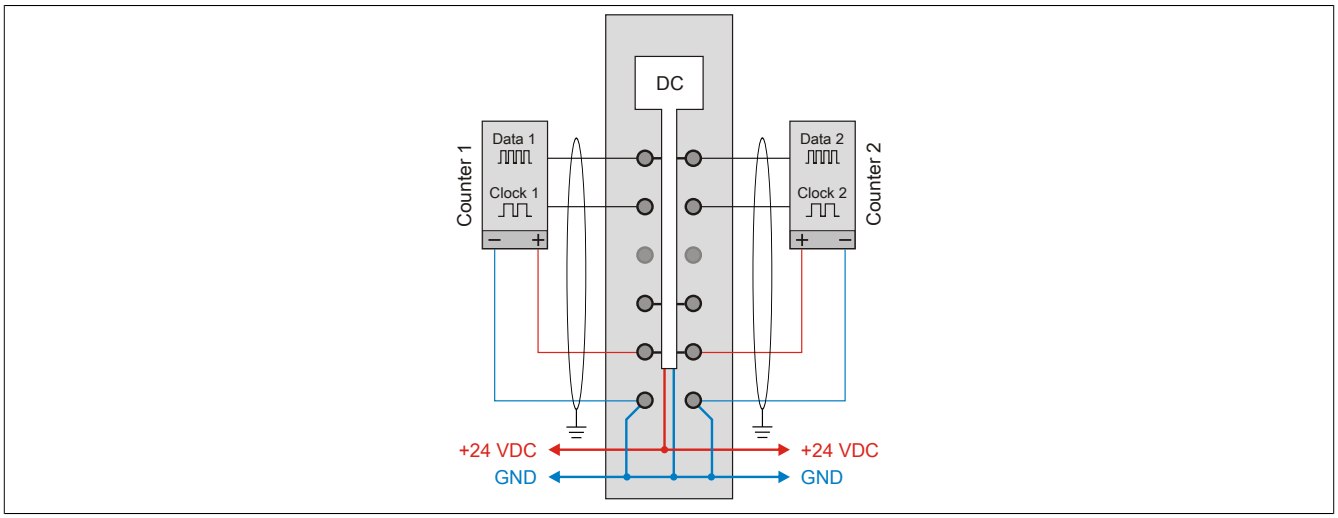
1) Depending on the configuration, a firmware update can take up to several minutes.

5 Pinout

Shielded cables must be used for all signal lines.

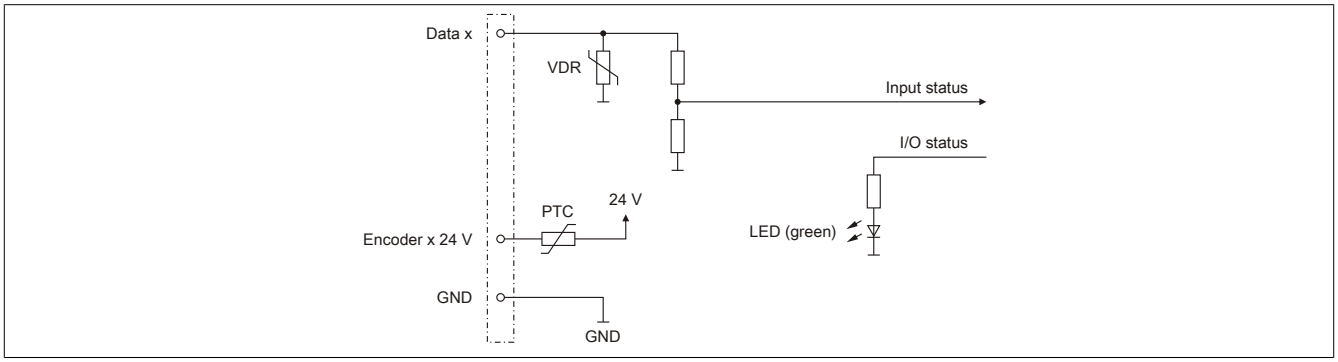


6 Connection example

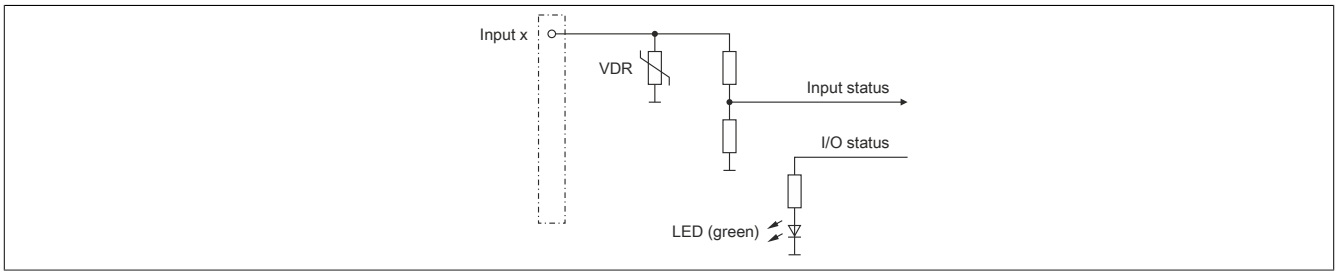


7 Input circuit diagram

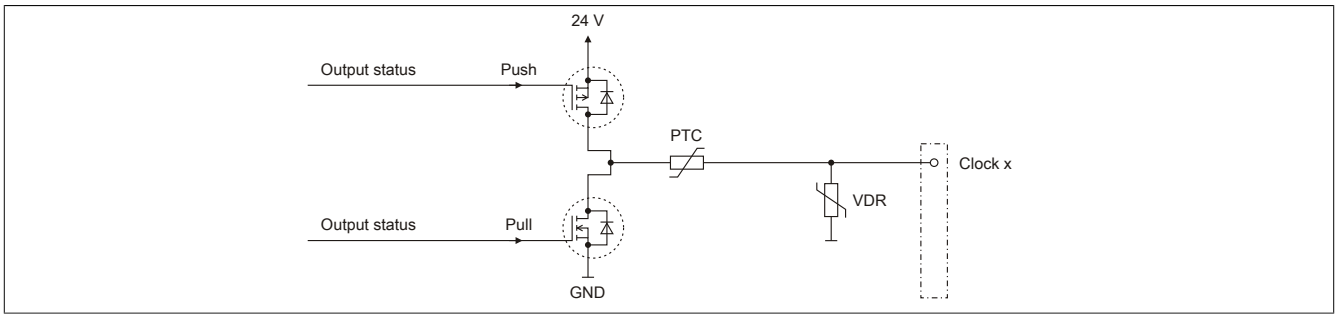
Counter inputs



Standard inputs



8 Output circuit diagram



9 Register description

9.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" of the X20 system user's manual.

9.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration						
7176	ConfigOutput15	UINT				•
7432	ConfigOutput16	UINT				•
7172	ConfigAdvanced01	UDINT				•
7428	ConfigAdvanced02	UDINT				•
Communication						
7184	Encoder01	UDINT	•			
7440	Encoder02	UDINT	•			
264	Input state of digital inputs 1 to 2	USINT	•			
	DigitalInput01	Bit 3				
	DigitalInput02	Bit 7				
40	Status of encoder supply	USINT	•			
	PowerSupply01	Bit 0				

9.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration							
7176	-	ConfigOutput15	UINT				•
7432	-	ConfigOutput16	UINT				•
7172	-	ConfigAdvanced01	UDINT				•
7428	-	ConfigAdvanced02	UDINT				•
Communication							
7184	0	Encoder01	UDINT	•			
7440	8	Encoder02	UDINT	•			
264	4	Input state of digital inputs 1 to 2	USINT	•			
		DigitalInput01	Bit 3				
		DigitalInput02	Bit 7				
40	5	Status of encoder supply	USINT	•			
		PowerSupply01	Bit 0				

1) The offset specifies the position of the register within the CAN object.

9.3.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use additional registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" of the X20 user's manual (version 3.50 or later).

9.3.2 CAN I/O bus controller

The module occupies 2 analog logical slots on CAN I/O.

9.4 SSI encoder configuration register

9.4.1 Standard configuration

Name:
ConfigOutput15 to ConfigOutput 16

This configuration register is used to set the coding, the clock rate and the number of bits. Default = 0. This must be set once using an acyclic write command.

"ConfigOutput15": Configuration register for SSI encoder01 and
"ConfigOutput16": Configuration register for SSI encoder02

Data type	Values	Bus controller default setting
UINT	See the bit structure.	0

Bit structure:

Bit	Name	Value	Information
0 - 5	SSI value valid bits	x	Bus controller default setting: 0
6 - 7	Clock rate	11	125 kHz. Bus controller default setting: 0
8 - 13	SSI number of bits	x	Number of bits including leading zeros. Bus controller default setting: 0
14	Reserved	0	
15	Keying	0	Binary encoding (bus controller default setting)
		1	Gray coding

9.4.2 Extended configuration

Name:
ConfigAdvanced01 to ConfigAdvanced02

This configuration register is used to set the coding, the clock rate, the number of bits and the monostable multivibrator settings. This must be set once using an acyclic write command.

It only differs from register "ConfigOutput15 + 16" on page 6 by data length and additional monostable multivibrator testing.

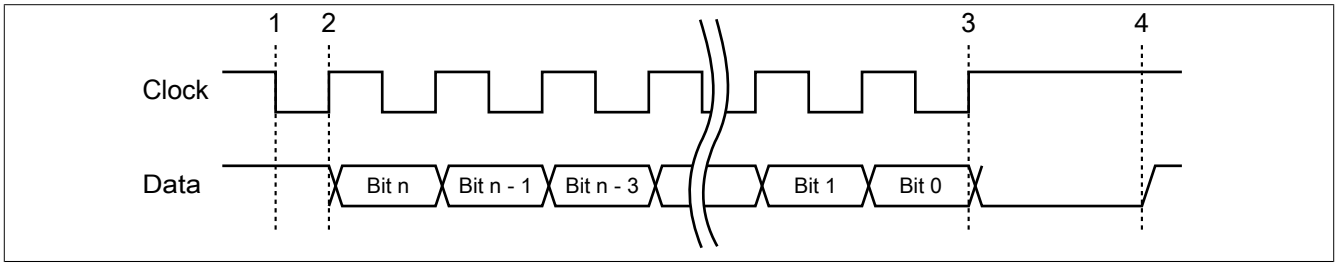
"ConfigAdvanced01": Configuration register for SSI encoder01 and
"ConfigAdvanced02": Configuration register for SSI encoder02

Data type	Values	Bus controller default setting
UDINT	See the bit structure.	65536

Bit structure:

Bit	Name	Value	Information
0 - 5	SSI value valid bits	x	Bus controller default setting: 0
6 - 7	Clock rate	11	125 kHz. Bus controller default setting: 0
8 - 13	SSI number of bits	x	Number of bits including leading zeros. Bus controller default setting: 0
14	Reserved	0	
15	Keying	0	Binary encoding (bus controller default setting)
		1	Gray coding
16 - 17	Monostable multivibrator	00	Check OFF, no additional clock bit
		01	Check set to high level (bus controller default setting)
		10	Check set to Low level
		11	Level is clocked but ignored
18 - 31	Reserved	0	

Transfer to synchronous serial interface



Measurement value processing

1) Starting bit ... Stores the measurement value
2) Output of first data bit
3) All data bits are transferred, monostable multivibrator time starts counting down.
4) Monostable multivibrator returns to its initial state. A new transfer can be started.

9.5 SSI encoder - Configuration registers

9.5.1 SSI position values

Name:
Encoder01 to Encoder02

The two SSI encoder values are displayed as 32-bit position values. The SSI position values are generated synchronously with the X2X cycle.

Data type	Value	Filter
UDINT	0 to 4,294,967,729	SSI position

9.5.2 Input state of digital inputs 1 to 2

Name:
DigitalInput01 to DigitalInput02

This register is used to indicate the input state of digital inputs 1 to 2.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
3	DigitalInput01	0 or 1	Input state - Digital input 1
7	DigitalInput02	0 or 1	Input state - Digital input 2

9.5.3 Status of encoder supply

Name:
PowerSupply01

This register shows the status of the integrated encoder supply. A faulty encoder power supply is displayed as a warning.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	PowerSupply01	0	24 VDC encoder power supply OK
		1	24 VDC encoder power supply faulty
1 - 7	Reserved	-	

9.6 Minimum cycle time

The minimum cycle time specifies the time up to which the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
128 µs

9.7 Maximum cycle time

The maximum cycle time defines how far the bus cycle can be increased without internal counter overflows causing module malfunctions.

Minimum cycle time
16 ms

9.8 Minimum I/O update time

The minimum I/O update time specifies how far the bus cycle can be reduced so that an I/O update is performed in each cycle.

Minimum I/O update time
128 µs