1.1 DI140

1.1.1 General Information

The DI140 digital input module is a screw-in module for the B&R SYSTEM 2003 and for the B&R Power Panel. It has 10 inputs for 24 VDC, four of which are equipped with counter functions. The counter inputs can be configured either as encoder or event counter inputs. The DI140 supports TPU functionality. The module is also equipped with supply voltage monitoring.

1.1.2 Order Data

Model Number	Short Description	Image
7DI140.70	2003 digital input module, 10 inputs 24 VDC, sink, 2 inputs for event counter operation or for direction dependent position determination, input frequency 50 kHz, 4 inputs can be used as high speed inputs (e. g. gate, frequency measurement), screw-in module. Order TB712 terminal block separately.	
7TB712.9	Terminal block, 12 pin, screw clamps	
7TB712.91	Terminal block, 12 pin, cage clamps	
7TB712:90-02	Terminal block, 12 pin, 20 pcs., screw clamps	
7TB712:91-02	Terminal block, 12 pin, 20 pcs., cage clamps	
Terminal block is not included in the delivery.		

Table 1: DI140 order data

1.1.3 Technical Data

Product ID	DI140
General Information	
C-UL-US Listed	In preparation
B&R ID Code	$4A
Module Type	B&R 2003 screw-in module
Slot	AF101 adapter module, CP interface Power Panel interface
Status Display	None
Power Consumption	Max. 0.4 W
Environment Temperature during Operation	5 °C to 55 °C
Inputs	
Number of Inputs	10
Design	IEC1131 - Type 1

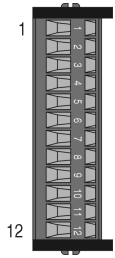
Table 2: DI140 technical data

Product ID	DI140
Wiring	Sink
Input Voltage Minimum Nominal Maximum	 18 VDC 24 VDC 30 VDC
Switching Threshold LOW HIGH	 < 5 V > 15 V
Input Current Inputs 1 -7 Inputs 8 -10	 8 mA @ 24 VDC 5 mA @ 24 VDC
Input Delay Inputs 1 -7 Inputs 8 -10	 Max. 3 µs Max. 1.3 ms
Electrical Isolation	Input - PLC
Incremental Encoder	
Signal Form	Square wave pulse
Evaluation	4x
Input Frequency	50 kHz
Count Frequency	200 kHz
Phase Offset between Channel A and B	90° ±25°
Counter Size	32-bit
Inputs Input 5 Input 6 Input 7 Input 8	 Channel A Channel B Reference pulse R Reference enable switch
Event Counter	
Signal Form	Square wave pulse
Input Frequency	100 kHz
Counter Size	32-bit
Inputs Input 5 Input 6	 Counter 1 Counter 2
Mechanical Characteristics	
Dimensions	B&R 2003 screw-in module

Table 2: DI140 technical data (cont.)

1.1.4 Pin Assignments

DI140 Pin Assignment	
Pin	**Assignment**
1	Input 1 (TPU)
2	Input 2 (TPU)
3	Input 3 (TPU)
4	Input 4 (TPU)
5	Input 5 / Encoder Channel A / Event Counter 1
6	Input 6 / Encoder Channel B / Event Counter 2
7	Input 7 / Reference Pulse
8	Input 8 / Reference Enable
9	Input 9
10	Input 10
11	+24 VDC Supply for Inputs
12	GND



TB712

Table 3: DI140 pin assignment

1.1.5 Connection Example

Wiring Example for Event Counter Operation

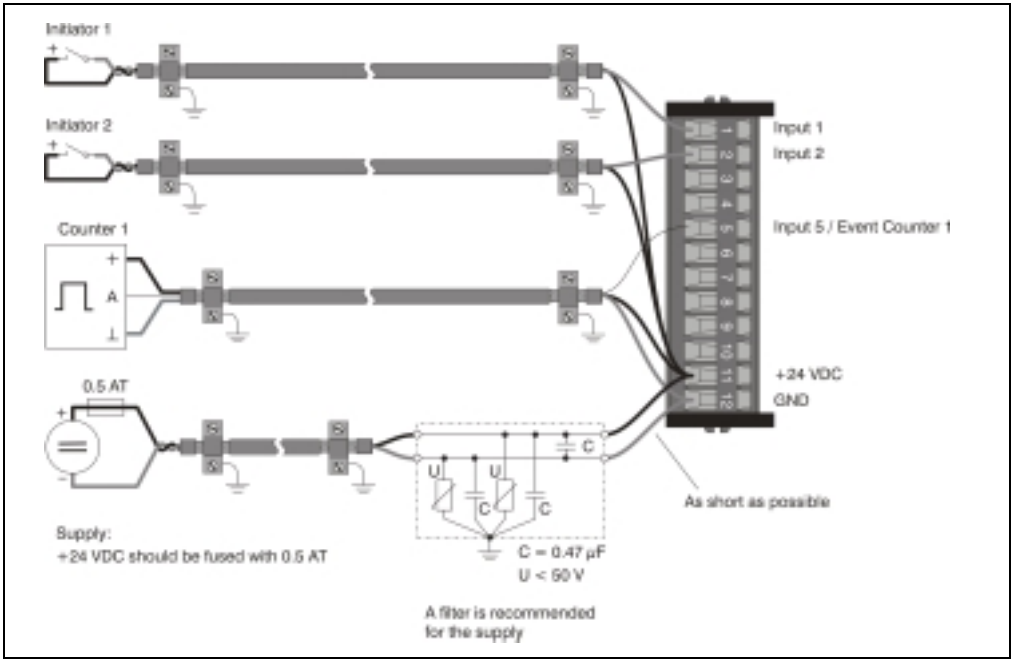


Figure 1: DI140 wiring example for event counter operation

The input delay of the high speed inputs is very short, therefore even low levels of disturbance on the supply can cause the input level to be incorrect. For this reason, a protective circuit in the supply line, similar to the one in the wiring example, is recommended. The varistors protect the bypass capacitor.

Wiring Example for Incremental Encoder Operation (encoder connection)

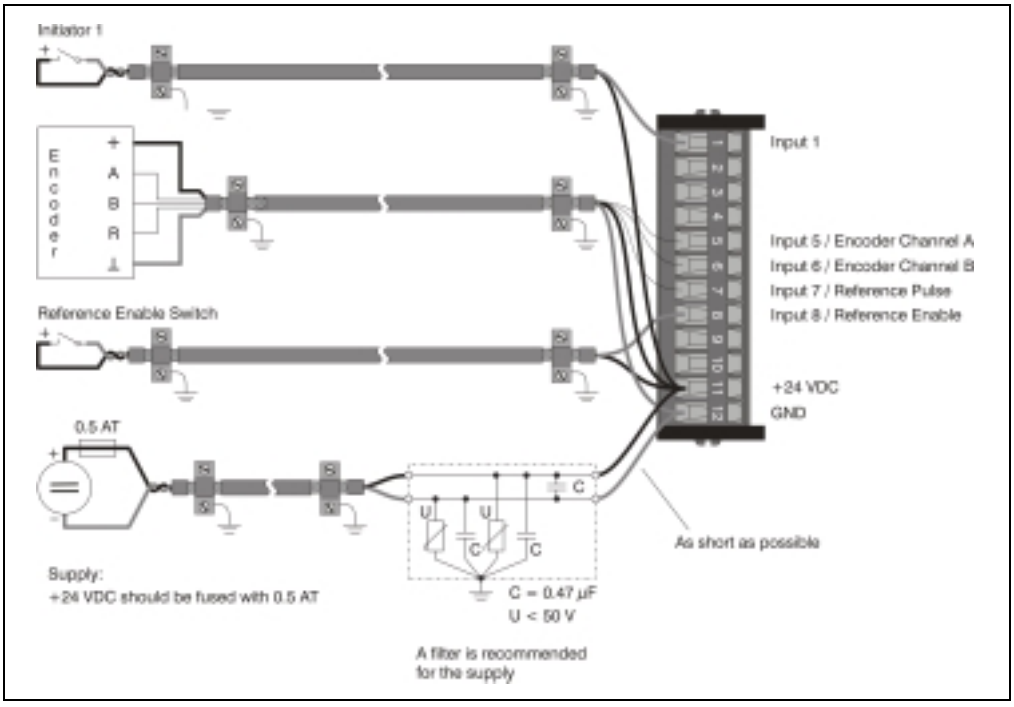


Figure 2: DI140 wiring example for incremental encoder operation (encoder connection)

The input delay of the high speed inputs is very short, therefore even low levels of disturbance on the supply can cause the input level to be incorrect. For this reason, a protective circuit in the supply line, similar to the one in the wiring example, is recommended. The varistors protect the bypass capacitor.

1.1.6 Input Circuit Diagram

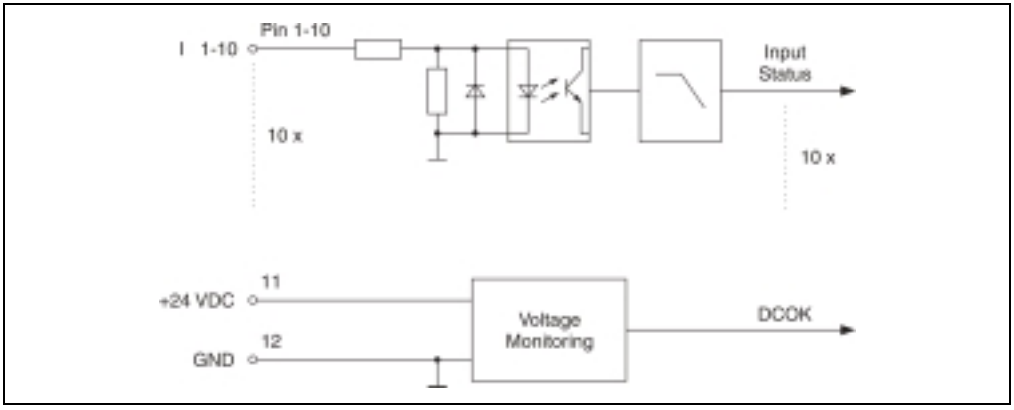


Figure 3: DI140 input circuit diagram

1.1.7 Area of Use

The DI140 is primarily a digital add-on module for the Power Panel, but it can also be used to increase the digital component density on the B&R 2003 system. Because of the number of digital inputs, the module presents itself to the system as an analog module; digital bit information is packed in the ‘analog value’ and must be extracted from the application.

1.1.8 Variable Declaration for Incremental Encoder Operation

The variable declaration is valid for the following controllers:

- CPU for the PLC 2003
- Remote I/O bus controller
- CAN bus controller

After booting, the DI140 digital module corresponds logically to an analog module. Communication takes place using shovel instructions from data and configuration words.

Accessing screw-in modules is also explained in the sections "AF101" and "CPU".

Incremental Encoder Operation with PLC 2003 CPU and Remote Slave

The following table provides an overview of the data and configuration words that are used for this module.

Data Access	VD Data Type	VD Module Type	VD Chan.	R	W	Description
Data Word 0	UINT	Transp. In	0	●		Input states
Data Word 1	UINT	Transp. In	2	●		Module status
Data Word 2	DINT	Transp. In	4	●		Counter value
Configuration Word 4	DINT	Transp. In	8	●		Latch register 0 counter value
	UINT	Transp. Out	8		●	Latch condition, latch 0
Configuration Word 5	UINT	Transp. Out	10		●	Latch condition, latch 1
Configuration Word 6	DINT	Transp. In	12	●		Latch register 1 counter value
	DINT	Transp. Out	12		●	Reference position
Configuration Word 8	UINT	Transp. Out	16		●	Latch and reference request
Configuration Word 12	UINT	Transp. In	24	●		Module status (current status unlatched)
Configuration Word 14	UINT	Transp. In	28	●		Module type
	UINT	Transp. Out	28		●	Module configuration

Table 4: DI140 data and configuration words for incremental encoder with CPU and remote slave

Incremental Encoder Operation with CAN Slaves

The following table provides an overview of the data and configuration words that are used for this module.

Data Access	VD Data Type	VD Module Type	VD Chan.	R	W	Description
Data Word 0	DINT	Transp. In	0	●		Counter value
Data Word 2	UINT	Transp. In	4	●		Module status
Data Word 3	UINT	Transp. In	6	●		Input states
Configuration Word 4	DINT	Transp. In	8	●		Latch register 0 counter value
	UINT	Transp. Out	8		●	Latch condition, latch 0
Configuration Word 5	UINT	Transp. Out	10		●	Latch condition, latch 1
Configuration Word 6	DINT	Transp. In	12	●		Latch register 1 counter value
	DINT	Transp. Out	12		●	Reference position
Configuration Word 8	UINT	Transp. Out	16		●	Latch and reference request
Configuration Word 12	UINT	Transp. In	24	●		Module status (current status unlatched)
Configuration Word 14	UINT	Transp. In	28	●		Module type
	UINT	Transp. Out	28		●	Module configuration

Table 5: DI140 data and configuration words for incremental encoder with CAN slave

Note:

B&R 2000 users have to exchange the two counter status words so that the high word is first (Motorola format)!

Access using CAN Identifier

Access via CAN identifiers is used if the slave is being controlled by a device from another manufacturer. Access via CAN identifiers is described in an example in . The transfer modes are explained in .

Data cannot be packed on the DI140. Therefore one CAN object is transferred per screw-in module. If an adapter module AF101 is equipped with a four DI140 modules, the CAN object has the following structure:

Slot	CAN ID [1]	Word 1		Word 2		Word 3		Word 4	
1	542	Counter LL	Counter ML	Counter MH	Counter HH	Status L	Status H	Inputs L	Inputs H
2	543	Counter LL	Counter ML	Counter MH	Counter HH	Status L	Status H	Inputs L	Inputs H
3	544	Counter LL	Counter ML	Counter MH	Counter HH	Status L	Status H	Inputs L	Inputs H
4	545	Counter LL	Counter ML	Counter MH	Counter HH	Status L	Status H	Inputs L	Inputs H

Table 6: DI140 CAN objects for incremental encoder operation

1) CAN ID = 542 + (nn - 1) x 16 + (ma - 1) x 4 + (sl - 1)
nn .... Node number of the CAN slaves = 1
ma ... Module address of the AF101 = 1
sl ..... Slot number of the screw-in module on the AF101 (1 - 4)

Note:

B&R 2000 users have to exchange the data so that the high data is first (Motorola format)!

For more information on ID allocation, see

Description of Data and Configuration Words

Data Word 0 (read)

Input states.

Bit	Description
0	Input 1
1	Input 2
2	Input 3
3	Input 4
4	Input 5
5	Input 6
6	Input 7
7	Input 8
8	Input 9
9	Input 10
10 - 15	Not defined, masked out

Data Word 1 (read)

Data word 1 includes the module status time constant for the counter value.

Bit	Description
0 [1)]	0 ... Counter value not taken 1 ... Counter value is taken in latch register 0
1 [1)]	0 ... Counter value not taken 1 ... Counter value is taken in latch register 1
2 - 6	Not defined, masked out
7 [1)]	0 ... Incremental encoder not referenced 1 ... Incremental encoder is referenced
8	0 ... Supply voltage for inputs is in the valid range 1 ... Supply voltage for inputs is too small
9 - 15	Not defined, masked out

1) These bits confirm a latch or reference request (see Section "Configuration Word 8 (write)", on page 14). If this request is deactivated, then these bits are reset again.

Data Word 2 (read)

Counter Value MSW.

Data Word 3 (read)

Counter Value LSW.

Configuration Words 4 and 5 (read)

Latch Register 0 for Counter Value:

Configuration Word	Counter Value
4	MSW
5	LSW

When latch request 0 is active (see Section "Configuration Word 8 (write)", on page 14), the counter value of the incremental encoder is placed in latch register 0 (see Section "Configuration Words 4 and 5 (write)", on page 12) if latch condition 0 is met. Configuration words 4 and 5 can be read consistently if latch register 0 is confirmed (bit 0 = 1) in the module status.

Bit 0 is reset in module status, when the latch request is cleared.

Age of the Latch Value:

A defined amount of time passes from the moment latch condition 0 is met until the counter value is placed in latch register 0. This time period defines the age of the latch values.

The age is independent of the input delay and of the processing time. It lies within the following range :

$$(\text{Input delay} - 400\ \mu s) < T_{Latch} < (\text{Input delay} + 400\ \mu s)$$

Configuration Words 4 and 5 (write)

The latch condtions for latch register 0 and 1 are defined with configuration words 4 and 5.

Configuration Word	Latch Register
4	0
5	1

A comparison value can be defined for inputs 1 to 8. The definition for the inputs, which is used for a latch condition, is made with bits 8 to 15. The counter value is latched as soon as the respective input has accepted the state of the comparison value.

Bit	Description
0	Comparison value for input 1
1	Comparison value for input 2
2	Comparison value for input 3
3	Comparison value for input 4
4	Comparison value for input 5
5	Comparison value for input 6
6	Comparison value for input 7
7	Comparison value for input 8
8	0 ... Input 1 not used for latch conditon 1 ... Latch condition with input 1
9	0 ... Input 2 not used for latch conditon 1 ... Latch condition with input 2
10	0 ... Input 3 not used for latch conditon 1 ... Latch condition with input 3
11	0 ... Input 4 not used for latch conditon 1 ... Latch condition with input 4
12	0 ... Input 5 not used for latch conditon 1 ... Latch condition with input 5
13	0 ... Input 6 not used for latch conditon 1 ... Latch condition with input 6
14	0 ... Input 7 not used for latch conditon 1 ... Latch condition with input 7
15	0 ... Input 8 not used for latch conditon 1 ... Latch condition with input 8

Configuration Words 6 and 7 (read)

Latch Register 1 for Counter Value:

Configuration Word	Counter Value
6	MSW
7	LSW

When latch request 1 is active (see Section "Configuration Word 8 (write)", on page 14), the counter value of the incremental encoder is placed in latch register 1 (see Section "Configuration Words 4 and 5 (write)", on page 12) if latch condition 1 is met. Configuration words 6 and 7 can be read consistently if the latch register 1 is confirmed (bit 1 = 1) in the module status.

Bit 1 is reset in module status, when the latch request is cleared.

Age of the Latch Value:

A defined amount of time passes from the moment latch condition 1 is met until the counter value is placed in latch register 1. This time period defines the age of the latch values.

The age is independent of the input delay and of the processing time. It lies within the following range:

$$(\text{Input delay} - 400\ \mu s) < T_{Latch} < (\text{Input delay} + 400\ \mu s)$$

Configuration Words 6 and 7 (write)

The reference position is defined with configuration words 6 and 7. The reference position is placed using referencing in data words 2 and 3.

Configuration Word	Reference Position
6	MSW
7	LSW

Configuration Word 8 (write)

Latch requests and referencing for the incremental encoder is activated with configuration word 8. Referencing mode is set in configuration word 14 using bits 0, 1 and 2.

Referencing Mode	Description
Direct Referencing	During direct referencing, the referencing position is applied immediately after setting the respective reference request in data words 2 and 3. After the reference position has been applied, the corresponding control bit is set in the module status. The control bit is cleared after the reference request has been reset.
Referencing with Reference Signals	When referencing using reference signals, inputs 7 and 8 are used. Input 7 ...Reference Pulse Input 8 ...Reference Enable: must be 1 (high), when bit 2 is set in configuration word 14. After setting the respective reference request and after receiving the reference pulse, the reference position is placed in data words 2 and 3. After the reference position has been applied, the corresponding control bit is set in the module status. The control bit is cleared after the reference request has been reset.

Bit	Description
0	0 ... No latch request 1 ... Latch request 0 activated on latch register 0
1	0 ... No latch request 1 ... Latch request 1 activated on latch register 1
2 - 6	0
7	0 ... Incremental encoder not referenced 1 ... Incremental encoder not referenced
8 - 15	0

Configuration Word 12 (read)

Configuration word 12 contains the module status (current status unlatched). The module status is written to data word 1.

Configuration Word 14 (read)

The high byte of configuration word 14 defines the module code.

Bit	Description
0 - 7	Not defined, masked out
8 - 15	Module Code: $4A

Configuration Word 14 (write)

The module is configured using configuration word 14.

Bit	Description
0	0 ... Referencing with reference signals Input 7 ... Reference pulse Input 8 ... Reference enable 1 ... Direct referencing. The reference position is placed immediately after the request in configuration word 8.
1	0 ... Referencing the falling edge of the reference pulse 1 ... Referencing the rising edge of the reference pulse
2	0 ... Reference enable not used 1 ... Reference enable linked with reference pulse
3 - 5	0
6	0 ... Count direction normal 1 ... Count direction inverted
7	1 ... Incremental Encoder Operation
8	The supply voltage for the digital inputs is monitored by the module. The status is shown by the module status in bit 8 and can be evaluated by the user. If a CAN bus controller is used, an alarm message is automatically generated by the bus controller when the permitted supply voltage range has not been reached. It corresponds to the alarm message "Measurement Range not reached" The generation of this alarm message can be deactivated by setting bit 8. The bit in the module status is processed further. 0 ... Alarm message for supply voltage monitoring is activated (when used with a CAN bus controller) 1 ... Supply voltage monitoring alarm message is deactivated
9 - 15	0

1.1.9 Variable Declaration for Event Counter Operation

The variable declaration is valid for the following controllers:

- CPU for the PLC 2003
- Remote I/O bus controller
- CAN bus controller

After booting, the DI140 digital module corresponds logically to an analog module. Communication takes place using shovel instructions from data and configuration words.

Accessing screw-in modules is also explained in the sections "AF101" and "CPU".

Event Counter Operation

The following table provides an overview of the data and configuration words that are used for this module.

Data Access	VD Data Type	VD Module Type	VD Chan.	R	W	Description
Data Word 0	UINT	Transp. In	0	●		Input states
Data Word 1	UINT	Transp. In	2	●		Module status
Data Word 2	UINT	Transp. In	4	●		Counter value of counter 1
Data Word 3	UINT	Transp. In	6	●		Counter value of counter 2
Configuration Word 4	UINT	Transp. In	8	●		Latch register 0, counter 1
	UINT	Transp. Out	8		●	Latch condition, latch 0
Configuration Word 5	UINT	Transp. In	10	●		Latch register 0, counter 2
	UINT	Transp. Out	10		●	Latch condition, latch 1
Configuration Word 6	UINT	Transp. In	12	●		Latch register 1, counter 1
	UINT	Transp. Out	12		●	Reference value, counter 1
Configuration Word 7	UINT	Transp. In	14	●		Latch register 1, counter 2
	UINT	Transp. Out	14		●	Reference value, counter 2
Configuration Word 8	UINT	Transp. Out	16		●	Latch and reference request
Configuration Word 12	UINT	Transp. In	24	●		Module status (current status unlatched)
Configuration Word 14	UINT	Transp. In	28	●		Module type
	UINT	Transp. Out	28		●	Module configuration

Table 7: DI140 data and configuration words for event counter operation

Access using CAN Identifier

Access via CAN identifiers is used if the slave is being controlled by a device from another manufacturer. Access via CAN identifiers is described in an example in . The transfer modes are explained in .

Data cannot be packed on the DI140. Therefore, one CAN object is transferred per screw-in module. If an adapter module AF101 is equipped with a four DI140 modules, the CAN object has the following structure:

Slot	CAN ID [1]	Word 1		Word 2		Word 3		Word 4	
1	542	Counter 2L	Counter 2H	Counter 1L	Counter 1H	Status L	Status H	Inputs L	Inputs H
2	543	Counter 2L	Counter 2H	Counter 1L	Counter 1H	Status L	Status H	Inputs L	Inputs H
3	544	Counter 2L	Counter 2H	Counter 1L	Counter 1H	Status L	Status H	Inputs L	Inputs H
4	545	Counter 2L	Counter 2H	Counter 1L	Counter 1H	Status L	Status H	Inputs L	Inputs H

Table 8: DI140 CAN objects event counter operation

1) CAN ID = 542 + (nn - 1) x 16 + (ma - 1) x 4 + (sl - 1)
nn .... Node number of the CAN slaves = 1
ma ... Module address of the AF101 = 1
sl ..... Slot number of the screw-in module on the AF101 (1 - 4)

Note:

B&R 2000 users have to exchange the data so that the high data is first (Motorola format)!

For more information on ID allocation, see

Description of Data and Configuration Words

Data Word 0 (read)

Input states.

Bit	Description
0	Input 1
1	Input 2
2	Input 3
3	Input 4
4	Input 5
5	Input 6
6	Input 7
7	Input 8
8	Input 9
9	Input 10
10 - 15	Not defined, masked out

Data Word 1 (read)

Data word 1 includes the module status time constant for the counter value.

Bit	Description
0 [1)]	0 ... Counter not applied 1 ... Counter is applied in latch register 0
1 [1)]	0 ... Counter not applied 1 ... Counter is applied in latch register 1
2 - 5	Not defined, masked out
6 [1)]	0 ... Counter 1 not referenced 1 ... Counter 1 is referenced
7 [1)]	0 ... Counter 2 not referenced 1 ... Counter 2 is referenced
8	0 ... Supply voltage for inputs is in the valid range 1 ... Supply voltage for inputs is too small
9 - 15	Not defined, masked out

1) These bits confirm a latch or reference request (see Section "Configuration Word 8 (write)", on page 22). If this request is deactivated, then these bits are reset again.

Data Word 2 (read)

Counter value of counter 1.

Data Word 3 (read)

Counter value of counter 2.

Configuration Words 4 and 5 (read)

Latch Register 0 for Counter 1 and 2:

When latch request 0 is active (see Section "Configuration Word 8 (write)", on page 22), both event counters are placed in latch register 0 (see Section "Configuration Words 4 and 5 (write)", on page 20) if latch condition 0 is met. Configuration words 4 and 5 can be read consistently if latch register 0 is confirmed (bit 0 = 1) in the module status.

Bit 0 is reset in module status, when the latch request is cleared.

Age of the Latch Value:

A defined amount of time passes from the moment latch condition 0 is met to the moment when both event counters are placed in latch register 0. This time period defines the age of the latch values.

The age is independent of the input delay and of the processing time. It lies within the following range :

$$(\text{Input delay} - 400\ \mu s) < T_{Latch} < (\text{Input delay} + 400\ \mu s)$$

Configuration Words 4 and 5 (write)

The latch condtions for latch register 0 and 1 are defined with configuration words 4 and 5.

Configuration Word	Latch Register
4	0
5	1

A comparison value can be defined for inputs 1 to 8. The definition for the inputs which are used for a latch condition, is made using bits 8 to 15.

Edge sensitive processing is used. That means that the counter value is latched the next time the respective input has accepted the status of the comparison value on the next occasion.

Bit	Description
0	Comparison value for input 1
1	Comparison value for input 2
2	Comparison value for input 3
3	Comparison value for input 4
4	Comparison value for input 5
5	Comparison value for input 6
6	Comparison value for input 7
7	Comparison value for input 8
8	0 ... Input 1 not used for latch conditon 1 ... Latch condition with input 1
9	0 ... Input 2 not used for latch conditon 1 ... Latch condition with input 2
10	0 ... Input 3 not used for latch conditon 1 ... Latch condition with input 3
11	0 ... Input 4 not used for latch conditon 1 ... Latch condition with input 4
12	0 ... Input 5 not used for latch conditon 1 ... Latch condition with input 5
13	0 ... Input 6 not used for latch conditon 1 ... Latch condition with input 6
14	0 ... Input 7 not used for latch conditon 1 ... Latch condition with input 7
15	0 ... Input 8 not used for latch conditon 1 ... Latch condition with input 8

Configuration Words 6 and 7 (read)

Latch Register 1 for Counter 1 and 2:

When latch request 1 is active (see Section "Configuration Word 8 (write)", on page 22), both event counters are placed in latch register 1 (see Section "Configuration Words 4 and 5 (write)", on page 20) if latch condition 1 is met. Configuration words 6 and 7 can be read consistently if latch register 1 is confirmed (bit 1 = 1) in the module status.

Bit 1 is reset in module status, when the latch request is cleared.

Age of the Latch Value:

A defined amount of time passes from the moment latch condition 1 is met to the moment when both event counters are placed in latch register 1. This time period defines the age of the latch values.

The age is independent of the input delay and of the processing time. It lies within the following range :

$$(\text{Input delay} - 400\ \mu s) < T_{Latch} < (\text{Input delay} + 400\ \mu s)$$

Configuration Words 6 and 7 (write)

Reference counter values are defined with configuration words 6 and 7. The reference counter values are placed using referencing in the data words 2 and 3.

Configuration Word	Reference Counter Value Status
6	Counter 1
7	Counter 2

Configuration Word 8 (write)

Latch requests and referencing for both counters is activated with configuration word 8. Referencing mode is set in configuration word 14 using bits 0 and 1.

Referencing Mode	Description
Direct Referencing	During direct referencing, the referencing counter status is taken immediately after setting the respective reference request in data word 2 and 3. After the reference value has been applied, the corresponding control bit is set in the module status. The control bit is cleared after the reference request has been reset.
Referencing with Reference Signals	When referencing using reference signals, inputs 7 and 8 are used. Input 7 ... Reference pulse Input 8 ... Reference enable, must be 1 (high) After setting the respective reference request and after receiving the reference pulse, the reference counter status is placed in data word 2 and 3. After the reference value has been applied, the corresponding control bit is set in the module status. The control bit is cleared after the reference request has been reset.

Bit	Description
0	0 ... No latch request 1 ... Latch request 0 activated on latch register 0
1	0 ... No latch request 1 ... Latch request 1 activated on latch register 1
2 - 5	0
6	0 ... Counter 1 not referenced 1 ... Counter 1 referenced
7	0 ... Counter 2 not referenced 1 ... Counter 2 referenced
8 - 15	0

Configuration Word 12 (read)

Configuration word 12 contains the module status (current status unlatched). The module status is written to data word 1.

Configuration Word 14 (read)

The high byte of configuration word 14 defines the module code.

Bit	Description
0 - 7	Not defined, masked out
8 - 15	Module Code: $4A

Configuration Word 14 (write)

The module is configured using configuration word 14.

Bit	Description
0	0 ... Referencing with reference signals Input 7 ... Reference pulse Input 8 ... Reference enable 1 ... Direct Referencing The reference value is placed in immediately after the request in configuration word 8.
1	0 ... Referencing the falling edge of the reference pulse 1 ... Referencing the rising edge of the reference pulse
2	0 ... Count at the rising edge 1 ... Count at the rising and falling edges
3 - 5	0
6	0 ... Up counter (0 → 65535), counters loop continuously 1 ... Down counter (65535 → 0), counters loop continuously
7	0 ... Event counter operation
8	The supply voltage for the digital inputs is monitored by the module. The status is shown by the module status in bit 8 and can be evaluated by the user. If a CAN bus controller is used, an alarm message is automatically generated by the bus controller when the permitted supply voltage range has not been reached. It corresponds to the alarm message "Measurement Range not reached" The generation of this alarm message can be deactivated by setting bit 8. The bit in the module status is processed further. 0 ... Alarm message for supply voltage monitoring is activated (when used with a CAN bus controller) 1 ... Alarm message for supply voltage monitoring is deactivated (when used with a CAN bus controller)
9 - 15	0