X67BCG321.L12

1 General information

EtherCAT is an Ethernet-based fieldbus developed by Beckhoff. This protocol is suitable for both hard and soft real-time requirements in automation technology. In addition to a ring structure, which becomes logically necessary because of the summation frame telegram used, the EtherCAT technology also physically supports topologies such as line, tree, star (limited) and combinations of these topologies. B&R's X20BC80G3 (expandable bus controller module) and X20HB88G0 (standalone junction base module) are available for implementing these topologies.

EtherCAT slave devices take the data designated for them from a telegram as it is passing through the device. Input data is also added to the telegram as it is passing through. The bus controller allows X2X Link I/O modules to be coupled to EtherCAT and operated on any EtherCAT master system. A transition between IP20 and IP67 protection outside of the control cabinet is possible by arranging X20, X67 or XV modules one after the other as needed at distances up to 100 m.

Master systems without FoE (File access over EtherCAT) support require an appropriate configuration tool to transfer the configuration (optional).

- Fieldbus: EtherCAT
- 16 digital channels, configurable as inputs or outputs
- Auto-configuration of I/O modules
- I/O configuration and firmware update via the fieldbus (FoE)
- Integrated connection to local expansion via X2X Link for 250 additional modules
- Full support of the modular slice concept via CoE (CANopen over EtherCAT)
- Configurable I/O cycle (0.2 to 4 ms)
- Synchronization between the fieldbus and X2X Link

Information:

Only the standard function model (see the respective module description) is supported when the bus controller is used together with multi-function modules it has automatically configured itself.

All other function models are supported when configured accordingly in Automation Studio V4.3 or later.

Automation Studio can be downloaded at no cost from the B&R website (www.br-automation.com). The evaluation license is permitted to be used to create complete configurations for fieldbus bus controllers at no cost.

2 Order data

Order number	Short description	Figure
	Bus controller modules	
X67BCG321.L12	X67 bus controller, 1 EtherCAT interface, X2X Link power supply 15 W, 16 digital channels configurable as inputs or outputs, 24 VDC, 0.5 A, configurable input filter, 2 event counters 50 kHz, M12 connectors, high-density module	

Required accessories
See "Required cables and connectors" on page 6.
For a general overview, see section "Accessories - General overview" of the X67 system user's manual.

3 Technical data

Order number	X67BCG321.L12
Short description	
Bus controller	EtherCAT
General information	
Inputs/Outputs	16 digital channels, configurable as inputs or outputs using Automation Studio or data point, inputs with additional functions
Isolation voltage between channel and bus	500 V_{eff}
Nominal voltage	24 VDC
B&R ID code	
Bus controller	0xACF8
Internal I/O module	0xB402
Sensor/Actuator power supply	0.5 A summation current
Status indicators	I/O function per channel, supply voltage, bus function
Diagnostics	
Outputs	Yes, using LED status indicator and software
I/O power supply	Yes, using LED status indicator and software
Connection type	
Fieldbus	M12, D-coded
X2X Link	M12, B-coded
Inputs/Outputs	8x M12, A-coded
I/O power supply	M8, 4-pin
Power output	15 W X2X Link power supply for I/O modules
Power consumption	
Fieldbus	2.5 W
Internal I/O	0.5 W
X2X Link power supply	15% of the power output for X2X Link
Additional power dissipation caused by actuators (resistive) [W]	0.6
Certifications	
CE	Yes
KC	Yes
EAC	Yes
UL	cULus E115267 Industrial control equipment
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5
ATEX	Zone 2, II 3G Ex nA IIA T5 Gc IP67, Ta = 0 - Max. 60°C TÜV 05 ATEX 7201X
Interfaces	
Fieldbus	EtherCAT slave
Variant	M12 interface (female) 2x on the module
Line length	Max. 100 m between 2 stations (segment length)
Transfer rate	100 Mbit/s
Transfer	
Physical layer	100BASE-TX
Half-duplex	Yes
Full-duplex	Yes
Autonegotiation	Yes
Auto-MDI / MDIX	Yes
Hub propagation delay	750 ns
Min. cycle time [1]	
Fieldbus	200 µs
X2X Link	200 µs
Synchronization between bus systems possible	Yes
I/O power supply	
Nominal voltage	24 VDC
Voltage range	18 to 30 VDC
Integrated protection	Reverse polarity protection
Power consumption	
Sensor/Actuator power supply	Max. 12 W [2]
Sensor/Actuator power supply	
Voltage	I/O power supply minus voltage drop for short-circuit protection
Voltage drop for short-circuit protection at 0.5 A	Max. 2 VDC
Summation current	Max. 0.5 A
Short-circuit proof	Yes
Digital inputs	
Input voltage	18 to 30 VDC
Input current at 24 VDC	Typ. 4 mA
Input characteristics per EN 61131-2	Type 1

Table 2: X67BCG321.L12 - Technical data

Order number	X67BCG321.L12
Input filter	
Hardware	≤10 µs (channels 1 to 4) / ≤70 µs (channels 5 to 16)
Software	Default 0 ms, configurable between 0 and 25 ms in 0.2 ms intervals
Input circuit	Sink
Additional functions	50 kHz event counting, gate measurement
Input resistance	Typ. 6 kΩ
Switching threshold	
Low	<5 VDC
High	>15 VDC
Event counter	
Quantity	2
Signal form	Square wave pulse
Evaluation	Each negative edge, cyclic counter
Input frequency	Max. 50 kHz
Counter 1	Input 1
Counter 2	Input 3
Counter frequency	Max. 50 kHz
Counter size	16-bit
Gate measurement	
Quantity	1
Signal form	Square wave pulse
Evaluation	Positive edge - Negative edge
Counter frequency	
Internal	48 MHz, 3 MHz, 187.5 kHz
Counter size	16-bit
Length of pause between pulses	≥100 µs
Pulse length	≥20 µs
Supported inputs	Input 2 or input 4
Digital outputs	
Variant	Current-sourcing FET
Switching voltage	I/O power supply minus residual voltage
Nominal output current	0.5 A
Total nominal current	8 A
Output circuit	Source
Output protection	Thermal shutdown in the event of overcurrent or short circuit, integrated protection for switching inductive loads, reverse polarity protection of the output power supply
Diagnostic status	Output monitoring with 10 ms delay
Leakage current when switched off	5 µA
Switching on after overload shutdown	Approx. 10 ms (depends on the module temperature)
$R_{DS(on)}$	150 mΩ
Residual voltage	<0.15 V at 0.5 A nominal current
Peak short-circuit current	<12 A
Switching delay	
0 → 1	<400 µs
1 → 0	<400 µs
Switching frequency	
Resistive load	Max. 100 Hz
Inductive load	See section "Switching inductive loads".
Braking voltage when switching off inductive loads	50 VDC
Electrical properties	
Electrical isolation	Bus isolated from EtherCAT and channel Channel not isolated from channel
Operating conditions	
Mounting orientation	
Any	Yes
Installation elevation above sea level	
0 to 2000 m	No limitation
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
Degree of protection per EN 60529	IP67
Ambient conditions	
Temperature	
Operation	-25 to 60°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Mechanical properties	
Dimensions	
Width	53 mm
Height	155 mm
Depth	42 mm

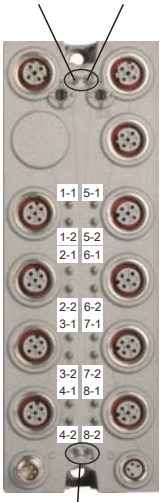
Table 2: X67BCG321.L12 - Technical data

Order number	X67BCG321.L12
Weight	370 g
Torque for connections	
M8	Max. 0.4 Nm
M12	Max. 0.6 Nm

Table 2: X67BCG321.L12 - Technical data

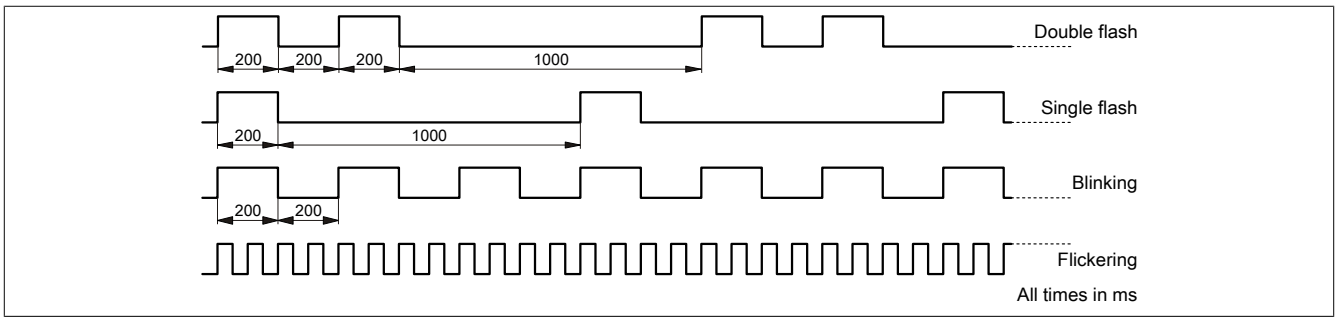
1) The minimum cycle time specifies the time up to which the bus cycle can be reduced without communication errors occurring.
2) The power consumption of the sensors and actuators connected to the module is not permitted to exceed 12 W.

4 LED status indicators

Figure	LED	Color	Status	Description
Status indicator 1: Left: L/A IF1, Right: S/E  Status indicator 2: Left: Green, Right: Red	**Status indicator 1:** Status indicator for Ethernet activity			
	L/A IF[1] (Link/Active)	Status indicator for Ethernet activity.		
		Green	Blinking	There is Ethernet activity (PORT OPEN) taking place on at least one of the EtherCAT connections.
			On	A connection has been established on at least one of the EtherCAT connections. However, there is no communication taking place (PORT OPEN).
			Off	An Ethernet connection has not been established on any of the EtherCAT connections (PORT CLOSED)
	STATUS[2]	Status indicator for the EtherCAT bus controller.		
		Green (RUN)	On	State OPERATIONAL
			Blinking	State PRE-OPERATIONAL
			Single flash	State SAFE-OPERATIONAL
			Flickering	The bus controller has started and is not yet in state INIT or it is in state BOOTSTRAP (e.g. during firmware download).
			Off	State INIT
		Red (ERROR)	On	A critical communication or application error has occurred.
			Blinking	Invalid configuration data
			Single flash	The bus controller has an internal error and has changed the EtherCAT state on its own.
			Double flash	Watchdog timeout (process data watchdog or EtherCAT watchdog)
			Flickering	Error in the start procedure (state INIT achieved but the error indicator bit in the AL status register is set)
			Off	No error
	I/O LEDs			
	1-1/2 to 8-1/2	Orange	-	Input/Output state of the corresponding channel.
	Status indicator 2: Status indicator for module functionality			
	Left	Green	Off	No power supplied to the module
			Single flash	Mode RESET
			Blinking	Mode PREOPERATIONAL
			On	Mode RUN
	Right	Red	Off	No power to module or everything OK
			On	Error or reset state
			Single flash	Warning/Error on an I/O channel. Level monitoring for digital outputs has been triggered.
			Double flash	Supply voltage not in the valid range

1) LED "L/A IF" shows the signals of the 2 EtherCAT interfaces combined (IN and OUT).
2) LED "STATUS" is a green/red dual LED used to indicate EtherCAT states ERROR (red) and RUN (green).

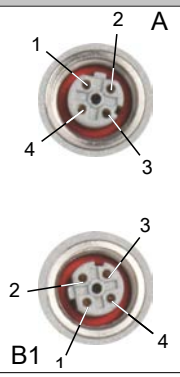
LED status indicators - Blink times



5 Operating and connection elements

6 Fieldbus interfaces

The module is connected to the network using pre-assembled cables. The connection is made using M12 circular connectors.

Connection	Pinout		
	Pin	Name	
	1	TXD	Transmit data
	2	RXD	Receive data
	3	TXD\	Transmit data\
	4	RXD\	Receive data\
	Shield connection made via threaded insert in the module		
	A → D-keyed (female), input B1 → D-keyed (female), output		

Information:

The color of the wires used in field-assembled cables for connecting to the fieldbus interface may deviate from the standard.

It is extremely important to make sure that the pinout is correct (see X67 section "Accessories - POWERLINK cables" in the X67 user's manual).

6.1 Cabling guidelines for bus controllers with Ethernet cables

Some X67 system bus controllers are based on Ethernet technology. POWERLINK cables supplied by B&R can be used for wiring.

Model number	Connection type
X67CA0E41.xxxx	Attachment cables - RJ45 to M12
X67CA0E61.xxxx	Connection cables - M12 to M12

The following cabling guidelines must be observed:

- Use Cat 5 SFTP cables.
- Observe the minimum cable bend radius (see data sheet for the cable).

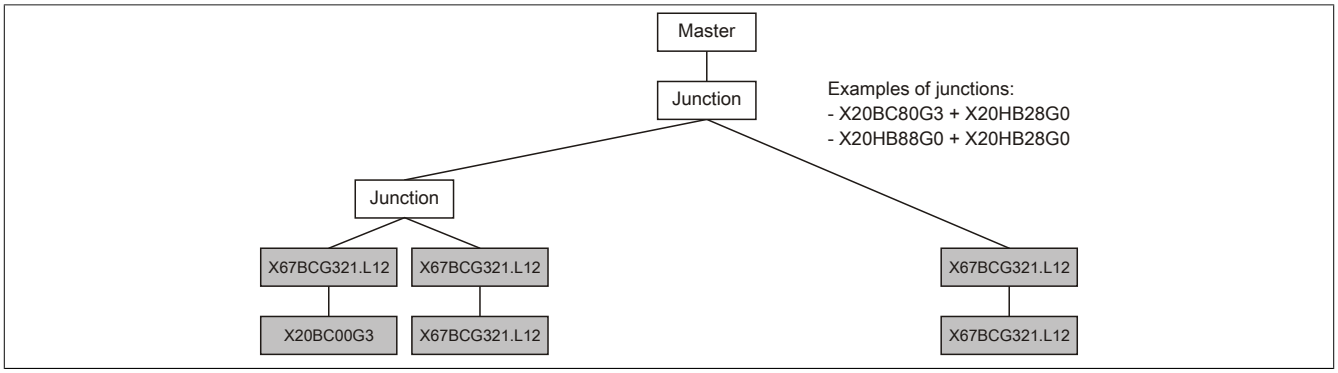
Information:

Using POWERLINK cables supplied by B&R (X67CA0E61.xxxx and X67CA0E41.xxxx) satisfies product standard EN 61131-2.

The customer must implement additional measures in the event of further requirements.

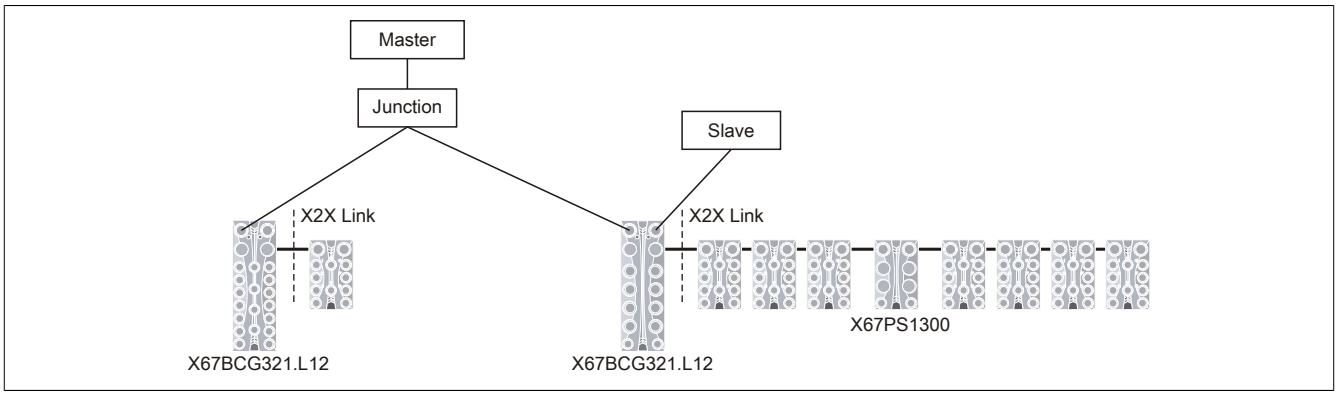
6.2 Integration into an EtherCAT network

This bus controller can be used in a tree or line topology as follows:



6.3 System configuration

A digital mixed module is already integrated in the bus controller. Up to 250 I/O modules can be connected to the bus controller.

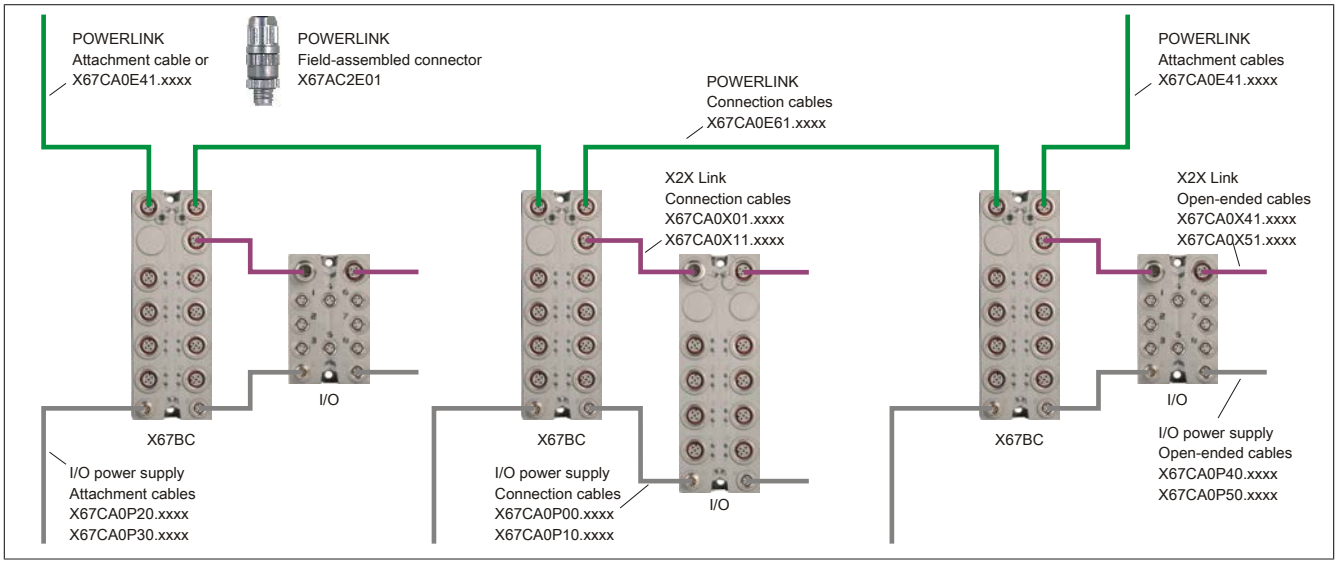


Information:

15 W are provided by the bus controller for additional X67 modules or other X2X Link-based modules.

System supply module X67PS1300 is needed for additional power. This system supply module provides 15 W for additional modules. Each one should be mounted in the middle of the modules that are to be supplied with power.

6.4 Required cables and connectors



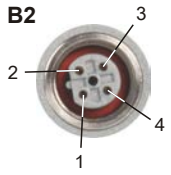
7 EtherCAT network address switches

Information:

The network address switches on this bus controller have no function.

8 X2X Link

Additional modules can be connected to the bus controller via X2X Link using pre-assembled cables. The connection is made using an M12 circular connector.

Connection	Pinout	
	**Pin**	**Name**
	1	X2X+
	2	X2X
	3	X2X⊥
	4	X2X\
	Shield connection made via threaded insert in the module	
	B2 → B-keyed (female), output	

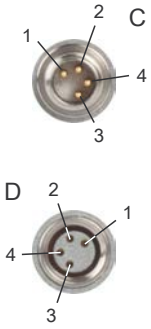
9 24 VDC I/O power supply

The I/O power supply is connected via M8 connectors C and D. The power supply is connected via connection C (male). Connector D (female) is used to route the power supply to other modules.

The fieldbus / X2X Link power supply and I/O power supply are supplied separately via pins 1 and 2.

Information:

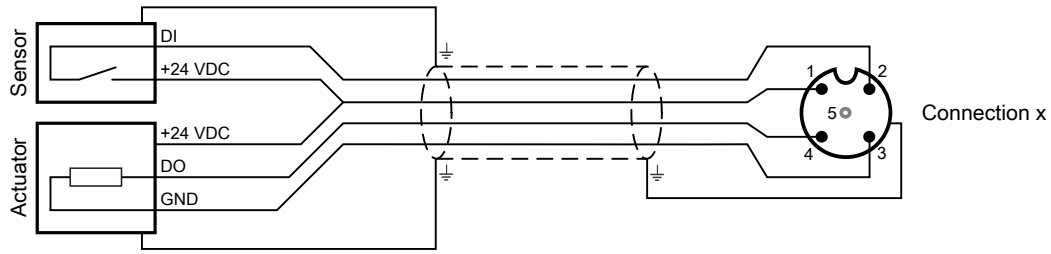
The maximum permissible current for the I/O power supply is 8 A (4 A per pin).

Connection	Pinout		
	**Pin**	**Connector C (male)**	**Connector D (female)**
	1	24 VDC fieldbus / X2X Link	24 VDC I/O
	2	24 VDC I/O	24 VDC I/O
	3	GND	GND
	4	GND	GND
	C → Connector (male) in module, feed for I/O power supply D → Connector (female) in module, routing of I/O power supply		

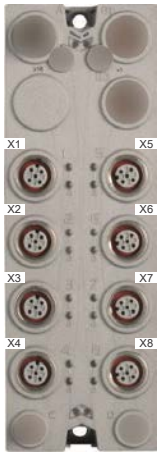
10 Integrated digital mixed module

1 additional mixed module can be saved by the digital mixed module integrated in the bus controller.

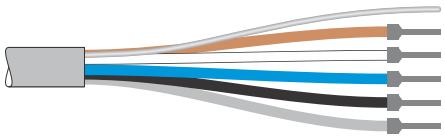
10.1 Connection example



10.2 Pinout



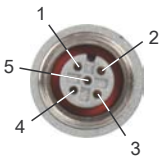
X1 to X8
M12 ①



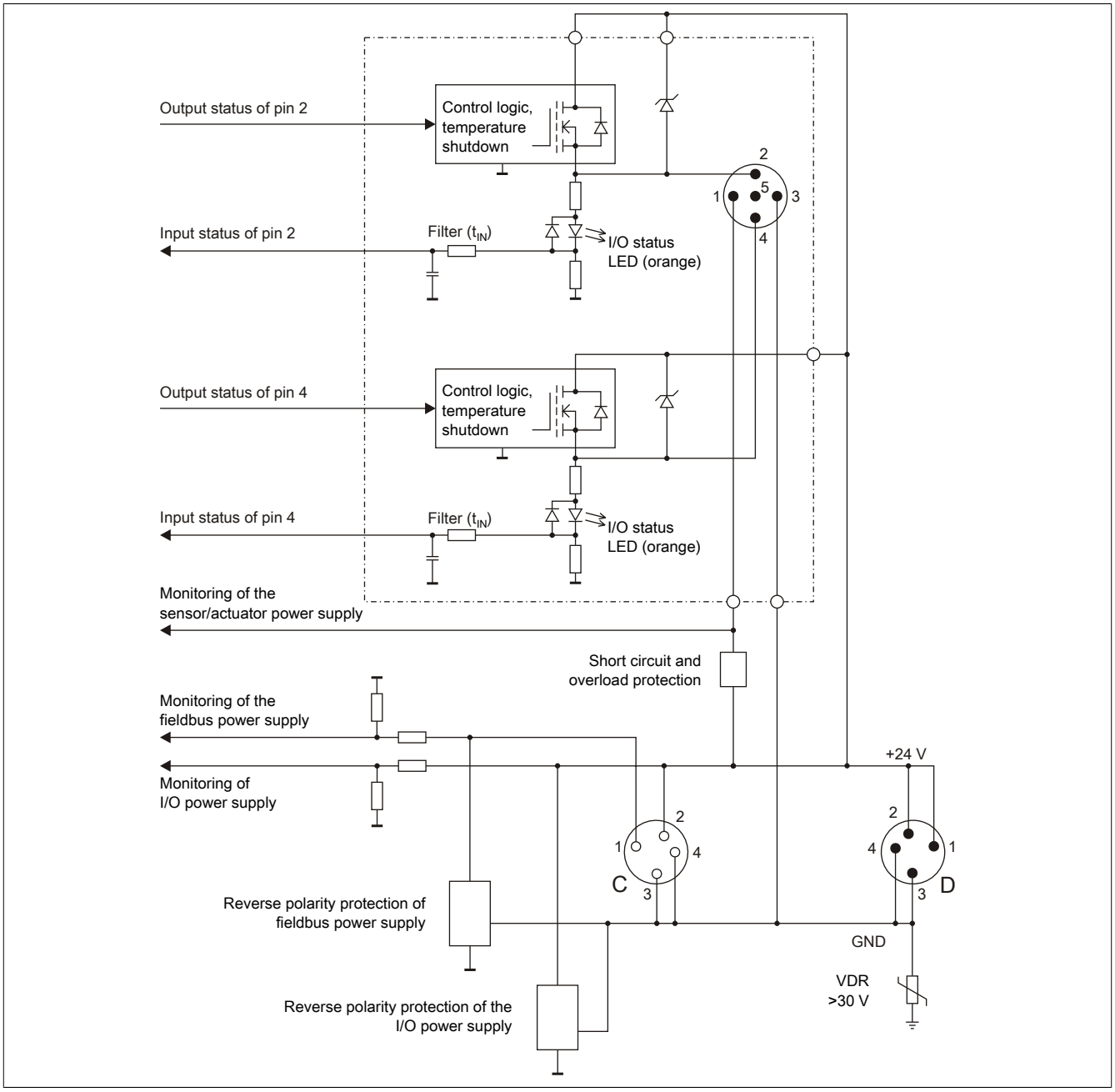
SHLD	
1	+24 VDC
2	DI/DO x-1
3	GND
4	DI/DO x-2
5	NC

① X67CA0A41.xxxx: M12 sensor cable, straight
X67CA0A51.xxxx: M12 sensor cable, angled

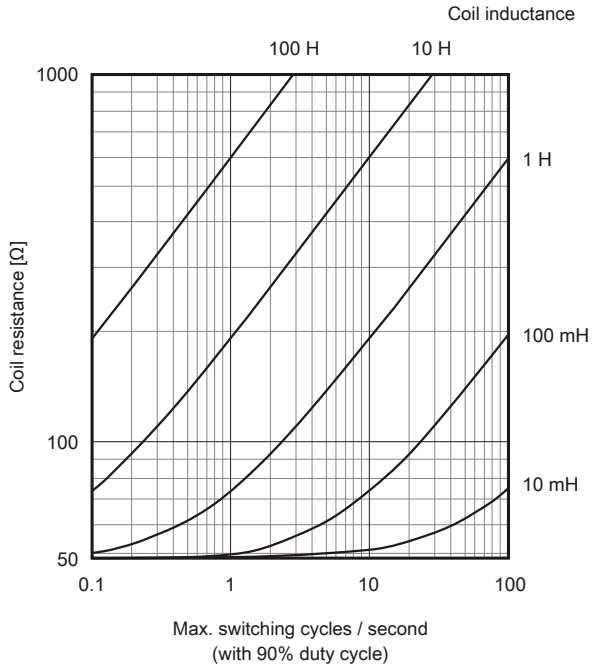
10.3 Connection X1 to X8

M12, 5-pin	Pinout	
Connection 1 to 4	**Pin**	**Name**
	1	24 VDC sensor/actuator power supply[1)]
	2	Input/Output x-1
	3	GND
	4	Input/Output x-2
	5	NC
Connection 5 to 8	Shield connection made via threaded insert in the module. 1) An external sensor/actuator power supply is not permitted. X1 to X8 → A-keyed (female), input/output	

10.4 Input/Output circuit diagram



10.5 Switching inductive loads



11 Register description

11.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" in the X67 system user's manual.

11.2 Function model 2 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration						
16	ConfigIOMask01	USINT				•
17	ConfigIOMask02	USINT				•
18	ConfigOutput03 (input filter)	USINT				•
Communication						
0	Input state of digital inputs 1 to 16	UINT	•			
	DigitalInput01	Bit 0				
	...	...				
	DigitalInput16	Bit 15				
2	Switching state of digital outputs 1 to 16	UINT			•	
	DigitalOutput01	Bit 0				
	...	...				
	DigitalOutput16	Bit 15				
30	Status of digital outputs 1 to 16	UINT	•			
	StatusDigitalOutput01	Bit 0				
	...	...				
	StatusDigitalOutput16	Bit 15				
26	Input latch - Rising edges 1 to 8	USINT	•			
	InputLatch01	Bit 0				
	...	...				
	InputLatch08	Bit 7				
27	Input latch - Rising edges 9 to 16	USINT	•			
	InputLatch09	Bit 0				
	...	...				
	InputLatch16	Bit 7				
28	Acknowledgment - Input latch 1 to 8	USINT			•	
	QuitInputLatch01	Bit 0				
	...	...				
	QuitInputLatch08	Bit 7				
29	Acknowledgment - Input latch 9 to 16	USINT			•	
	QuitInputLatch09	Bit 0				
	...	...				
	QuitInputLatch16	Bit 7				
8192	asy_ModulID	UINT		•		
8196	asy_SupplyStatus	USINT		•		
8208	asy_SupplyInput	USINT		•		
8210	asy_SupplyOutput	USINT		•		

11.3 Function model 1 - Counter

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration						
16	ConfigIOMask01	USINT				•
17	ConfigIOMask02	USINT				•
20	ConfigOutput01 (counter channel 1)	USINT				•
22	ConfigOutput02 (counter channel 2)	USINT				•
18	ConfigOutput03 (input filter)	USINT				•
Communication						
0	Input state of digital inputs 1 to 16	UINT	•			
	DigitalInput01	Bit 0				
	...	...				
	DigitalInput16	Bit 15				
2	Switching state of digital outputs 1 to 16	UINT			•	
	DigitalOutput01	Bit 0				
	...	...				
	DigitalOutput16	Bit 15				
30	Status of digital outputs 1 to 16	UINT	•			
	StatusDigitalOutput01	Bit 0				
	...	...				
	StatusDigitalOutput16	Bit 15				
26	Input latch - Rising edges 1 to 8	USINT	•			
	InputLatch01	Bit 0				
	...	...				
	InputLatch08	Bit 7				
27	Input latch - Rising edges 9 to 16	USINT	•			
	InputLatch09	Bit 0				
	...	...				
	InputLatch16	Bit 7				
28	Acknowledgment - Input latch 1 to 8	USINT			•	
	QuitInputLatch01	Bit 0				
	...	...				
	QuitInputLatch08	Bit 7				
29	Acknowledgment - Input latch 9 to 16	USINT			•	
	QuitInputLatch09	Bit 0				
	...	...				
	QuitInputLatch16	Bit 7				
4	Counter01	UINT	•			
6	Counter02	UINT	•			
20	Reset counter 1	USINT			•	
	ResetCounter01	Bit 5				
22	Reset counter 2	USINT			•	
	ResetCounter02	Bit 5				
8192	asy_ModulID	UINT		•		
8196	asy_SupplyStatus	USINT		•		
8208	asy_SupplyInput	USINT		•		
8210	asy_SupplyOutput	USINT		•		

11.4 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration							
16	-	ConfigIOMask01	USINT				•
17	-	ConfigIOMask02	USINT				•
20	-	ConfigOutput01 (counter channel 1)	USINT				•
22	-	ConfigOutput02 (counter channel 2)	USINT				•
18	-	ConfigOutput03 (input filter)	USINT				•
Communication							
0	0	Input state of digital inputs 1 to 16	UINT	•			
		DigitalInput01	Bit 0				
		...	...				
		DigitalInput16	Bit 15				
2	2	Switching state of digital outputs 1 to 16	UINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput16	Bit 15				
30	-	Status of digital outputs 1 to 16	UINT	•			
		StatusDigitalOutput01	Bit 0				
		...	...				
		StatusDigitalOutput16	Bit 15				
26	-	Input latch - Rising edges 1 to 8	USINT	•			
		InputLatch01	Bit 0				
		...	...				
		InputLatch08	Bit 7				
27	-	Input latch - Rising edges 9 to 16	USINT	•			
		InputLatch09	Bit 0				
		...	...				
		InputLatch16	Bit 7				
28	-	Acknowledgment - Input latch 1 to 8	USINT			•	
		QuitInputLatch01	Bit 0				
		...	...				
		QuitInputLatch08	Bit 7				
29	-	Acknowledgment - Input latch 9 to 16	USINT			•	
		QuitInputLatch09	Bit 0				
		...	...				
		QuitInputLatch16	Bit 7				
4	-	Counter01	UINT		•		
6	-	Counter02	UINT		•		
20	-	Reset counter 1	USINT			•	
		ResetCounter01	Bit 5				
22	-	Reset counter 2	USINT			•	
		ResetCounter02	Bit 5				
8192	-	asy_ModulID	UINT		•		
8196	-	asy_SupplyStatus	USINT		•		
8208	-	asy_SupplyInput	USINT		•		
8210	-	asy_SupplyOutput	USINT		•		

1) The offset specifies the position of the register within the CAN object.

11.4.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use other registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" in the X67 user's manual (version 3.30 or later).

11.4.2 CAN I/O bus controller

The module occupies 2 digital logical slots on CAN I/O.

11.5 Configuration

11.5.1 I/O mask 1 to 8

Name:
ConfigIOMask01

Channels are configured as inputs/outputs in this register. It also determines whether output monitoring or filtering is applied to the channels. Outputs are monitored but not filtered.

Information:

In counter operation, channels 1 to 4 can only be configured as inputs.

Data type	Values	Bus controller default setting
USINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0	Channel 1 configured as input/output	0	Configured as input (bus controller default setting)
		1	Configured as output
...		...	
7	Channel 8 configured as input/output	0	Configured as input (bus controller default setting)
		1	Configured as output

11.5.2 I/O mask 9 to 16

Name:
ConfigIOMask02

Channels are configured as inputs/outputs in this register. It also determines whether output monitoring or filtering is applied to the channels. Outputs are monitored but not filtered.

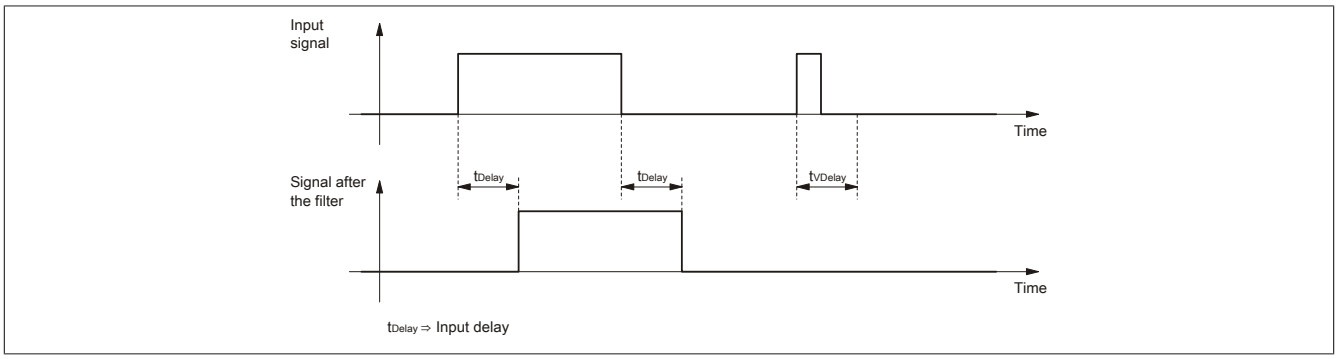
Data type	Values	Bus controller default setting
USINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0	Channel 9 configured as input/output	0	Configured as input (bus controller default setting)
		1	Configured as output
...		...	
7	Channel 16 configured as input/output	0	Configured as input (bus controller default setting)
		1	Configured as output

11.5.3 Input filter

An input filter is available for each input. The input delay can be set using register "ConfigOutput03" on page 15. Disturbance pulses which are shorter than the input delay are suppressed by the input filter.



11.5.3.1 Digital input filter

Name:
ConfigOutput03

This register can be used to specify the filter value for all digital inputs.

The filter value can be configured in steps of 100 µs. It makes sense to enter values in steps of 2, however, since the input signals are sampled every 200 µs.

Data type	Value	Filter
USINT	0	No software filter (bus controller default setting)
	2	0.2 ms
	...	...
	250	25 ms - Higher values are limited to this value

11.5.4 Configuration of Counter Channels 1 and 2

Name:
ConfigOutput01 to ConfigOutput02
ResetCounter01 to ResetCounter02

Counter channels 1 and 2 are configured in this register.

Data type	Values	Bus controller default setting
USINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0 - 2	Configuration of the counter frequency (only with gate measurement)	000	Counter frequency = 48 MHz (bus controller default setting)
		001	Counter frequency = 3 MHz
		010	Counter frequency = 187.5 kHz
		011 to 111	Reserved
3 - 4	Reserved	0	
5	ResetCounter0x	0	No affect on counter (bus controller default setting)
		1	Delete counter
6 - 7	Configuration of the operating mode	0	Event counter operation (Bus controller default setting)
		1	Gate measurement

Event counter operation

The falling edges are registered on the counter input.

The counter status is collected with a fixed offset to the network cycle and transferred in the same cycle.

Gate measurement

> **Information:**
>
> **Only one of the counter channels at a time can be used for gate measurement.**

The time of rising to falling edges for the gate input is registered using an internal frequency. The result is checked for overflow (0xFFFF).

The recovery time between measurements must be >100 µs.

The measurement result is transferred with the falling edge to the result memory.

11.6 Communication

11.6.1 Digital inputs

Unfiltered

The input state is collected with a fixed offset to the network cycle and transferred in the same cycle.

Filtered

The filtered status is collected with a fixed offset to the network cycle and transferred in the same cycle. Filtering takes place asynchronously to the network in multiples of 200 µs with a network-related jitter of up to 50 µs.

11.6.1.1 Input state of digital inputs 1 to 16

Name:
DigitalInput01 to DigitalInput16

This register indicates the input state of digital inputs 1 to 16.

Data type	Values
UINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	DigitalInput01	0 or 1	Input state - Digital input 1
...		...	
15	DigitalInput16	0 or 1	Input state - Digital input 16

11.6.2 Digital outputs

The output status is transferred to the output channels with a fixed offset in relation to the network cycle (SyncOut).

11.6.2.1 Switching state of digital outputs 1 to 16

Name:
DigitalOutput01 to DigitalOutput16

This register is used to store the switching state of digital outputs 1 to 16.

Data type	Values
UINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput01	0	Digital output 01 reset
		1	Digital output 01 set
...		...	
15	DigitalOutput16	0	Digital output 16 reset
		1	Digital output 16 set

11.6.3 Monitoring status of the digital outputs

On the module, the output states of the outputs are compared to the target states. The control of the output driver is used for the target state.

A change in the output state resets monitoring for that output. The status of each individual channel can be read. A change in the monitoring status is actively transmitted as an error message.

11.6.3.1 Status of digital outputs 1 to 16

Name:
StatusDigitalOutput01 to StatusDigitalOutput16

This register is used to indicate the status of digital outputs 1 to 16.

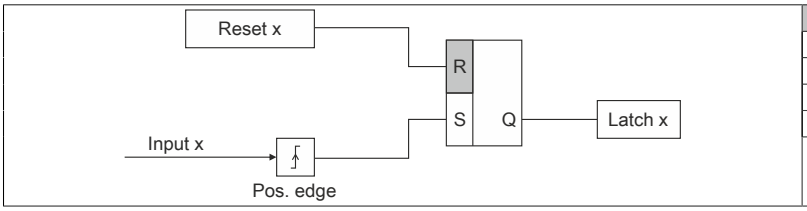
Data type	Values
UINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	StatusDigitalOutput01	0	Channel 01: No error
		1	Channel 01: Short circuit or overload
...		...	
15	StatusDigitalOutput16	0	Channel 16: No error
		1	Channel 16: Short circuit or overload

11.6.4 Input latch

It works in the same way as a dominant reset RS flip-flop.



R	S	Q	State
0	0	x	Do not change
0	1	1	Set
1	0	0	Reset
1	1	0	Reset

11.6.4.1 Input latch - Rising edges 1 to 8

Name:
InputLatch01 to InputLatch08

The rising edges of the input signal can be latched with a resolution of 200 µs in this register. The input latch is either reset or prevented from latching with register "QuitInputLatch0x" on page 18.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	InputLatch01	0	Do not latch input 1
		1	Latch input 1
...		...	
7	InputLatch08	0	Do not latch input 8
		1	Latch input 8

11.6.4.2 Input latch - Rising edges 9 to 16

Name:
InputLatch09 to InputLatch16

The rising edges of the input signal can be latched with a resolution of 200 µs in this register. The input latch is either reset or prevented from latching with register "QuitInputLatchxx" on page 18.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	InputLatch09	0	Do not latch input 9
		1	Latch input 9
...		...	
7	InputLatch16	0	Do not latch input 16
		1	Latch input 16

11.6.4.3 Acknowledgment - Input latch 1 to 8

Name:
QuitInputLatch01 to QuitInputLatch08

This register is used to reset the input latch by channel.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	QuitInputLatch01	0	Do not reset input 1
		1	Reset input 1
...		...	
7	QuitInputLatch08	0	Do not reset input 8
		1	Reset input 8

11.6.4.4 Acknowledgment - Input latch 9 to 16

Name:
QuitInputLatch09 to QuitInputLatch16

This register is used to reset the input latch by channel.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	QuitInputLatch09	0	Do not reset input 9
		1	Reset input 9
...		...	
7	QuitInputLatch16	0	Do not reset input 16
		1	Reset input 16

11.6.5 Event counter / Gate measurement

Name:
Counter01 and Counter02

Depending on the mode, this register contains the counter value or gate time of channel 1 and channel 2.

Data type	Values
UINT	0 to 65535

11.6.6 Reading the module ID

Name:
asy_ModulID

This register offers the possibility to read the module ID.

Data type	Values
UINT	Module ID

11.6.7 Operating limit status registers

Name:
asy_SupplyStatus

This register can be used to read the status of the operating limits.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Input supply within / outside of the warning limits	0	Within the warning limits (18 to 30 V)
		1	Outside of the warning limits (<18 V or >30 V)
1	Reserved	0	
2	Output supply within / outside of the warning limits	0	Within the warning limits (18 to 30 V)
		1	Outside of the warning limits (<18 V or >30 V)
3 - 7	Reserved	0	

11.6.8 I/O supply voltage

Name:
asy_SupplyInput

This register contains the I/O supply voltage measured by the module.

Data type	Values	Information
USINT	0 to 255	Resolution 1 V

11.6.9 Output supply voltage

Name:
asy_SupplyOutput

This register contains the output supply voltage measured by the module.

Data type	Values	Information
USINT	0 to 255	Resolution 1 V

11.7 Minimum I/O update time

The minimum I/O update time specifies how far the bus cycle can be reduced so that an I/O update is performed in each cycle.

	Minimum I/O update time
Without filtering	150 µs
With filtering	200 µs
Counter operation	250 µs

11.8 Minimum cycle time

The minimum cycle time specifies how far the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

	Minimum cycle time
Without filtering	150 µs
With filtering	200 µs
Counter operation	250 µs