X20MM4456

1 General information

The PWM motor bridge module is used to control 4 DC motors with a nominal voltage of 24 to 48 VDC ±25% at a nominal current up to 6 A. The module can be reconfigured and used in current controller mode for controlling inductive loads. The module is also equipped with 16 digital inputs, which can be used as incremental counters. The 4 motors are controlled with a full-bridge (H-bridge). This enables the motors to be moved in both directions.

- 4x outputs (H bridge) with PWM control and 24 to 48 VDC ±25% supply
- 6 A nominal current (10 A max current)
- 15 Hz to 50 kHz frequency, 16-bit
- PWM resolution, 15-bit, + sign, minimum 10 ns
- Configurable dither
- 4x 4 inputs 24V, can be configured as ABR
- Sink connection
- 1-wire connections

2 Order data

Order number	Short description	Figure
	Motor controllers	
X20MM4456	X20 PWM motor module, 24 to 48 VDC ±25%, 4 PWM motor bridges, 6 A continuous current, 10 A peak current, 4x 4 digital inputs 24 VDC, sink, configurable as incremental encoder	
	Required accessories	
	Terminal blocks	
0TB3103-7020	Accessory terminal block, 3-pin, screw clamps 6 mm²	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 1: X20MM4456 - Order data

3 Technical data

Order number	X20MM4456
Short description	
I/O module	4-channel PWM motor bridge, 4 ABR incremental encoders
General information	
B&R ID code	0xA177
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using LED status indicator and software
Output	Yes, using LED status indicator and software
I/O power supply	Yes, using software
Power consumption	
Bus	0.01 W
Internal I/O	2.4 W
External I/O 50 kHz	
24 VDC	3.3 W / channel
48 VDC	4.7 W / channel
60 VDC	5.4 W / channel
External I/O 10 kHz	
24 VDC	2.1 W / channel
48 VDC	2.4 W / channel
60 VDC	2.6 W / channel
External I/O 5 kHz	
24 VDC	2 W / channel
48 VDC	2.1 W / channel
60 VDC	2.2 W / channel
Additional power dissipation caused by actuators (resistive) [W]	-
Certifications	
CE	Yes
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X
UL	cULus E225616 Power conversion equipment
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5
EAC	Yes
KC	Yes
Digital inputs	
Quantity	16
Nominal voltage	24 VDC
Input characteristics per EN 61131-2	Type 1
Input voltage	24 VDC (-15% / +20%)
Input current at 24 VDC	Approx. 4 mA
Input circuit	Sink
Input filter	
Hardware	<5 µs
Software	-
Connection type	1-wire connections
Input resistance	Typ. 6 kΩ
Additional functions	4x ABR incremental encoder
Switching threshold	
Low	<5 VDC
High	>15 VDC
Insulation voltage between channel and bus	500 V_{eff}
ABR incremental encoder	
Quantity	4
Encoder inputs	24 V, asymmetrical
Counter size	16-bit
Input frequency	Max. 50 kHz
Evaluation	4x
Signal form	Square wave pulse
PWM output	
Quantity	4
Nominal voltage	24 to 48 VDC ±25% [1)]
Nominal current	6 A
Maximum current	10 A (2 s)
PWM frequency	15 Hz to 50 kHz

Table 2: X20MM4456 - Technical data

Order number	X20MM4456
Actuator power supply	
Supply	External
Fuse	Required line fuse: Max. 32 A slow-blow (see "Overcurrent protection")
Output protection	Thermal shutdown in the event of overcurrent or short circuit
Variant	H bridge
Configurable dither	Amplitude, frequency
Period duration resolution	16-bit, min. 20 µs
Phase shift PWM1, 2, 3, 4	90° each
DC bus capacitance	680 µF
PWM pulse width	
PWM mode	15 bits plus sign ≥10 ns
Current mode	15 bits plus sign ≥10 ns
Insulation voltage between channel and bus	500 V_{eff}
Electrical properties	
Electrical isolation	Channel isolated from bus Channel not isolated from channel
Operating conditions	
Mounting orientation	
Horizontal	Yes
Installation elevation above sea level	
0 to 2000 m	No limitation
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
Degree of protection per EN 60529	IP20
Ambient conditions	
Temperature	
Operation	
Horizontal mounting orientation	0 to 50°C
Vertical mounting orientation	Not permitted
Derating	-
Storage	-25 to 70°C
Transport	-25 to 70°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical properties	
Note	Order 2x terminal block X20TB12 separately. Order 1x terminal block 0TB3103-7020 separately.
Pitch	$87.5^{+0.2}$ mm

Table 2: X20MM4456 - Technical data

1) The tolerance value is composed of the voltage tolerances and permissible total AC voltage component with a peak value of 5% of the rated voltage.

4 LED status indicators

For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" in the X20 system user's manual.

Status LED, left

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1)]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	e + r	Red on / Green single flash		Invalid firmware
	1 - 8	Green		Input state of the corresponding digital input
	M1 + M2	Orange	On	The corresponding output is active

1) Depending on the configuration, a firmware update can take up to several minutes.

Status LED, right

Figure	LED	Color	Status	Description
	9 - 16	Green		Input state of the corresponding digital input
	M3 + M4	Orange	On	The corresponding output is active

5 Connection elements

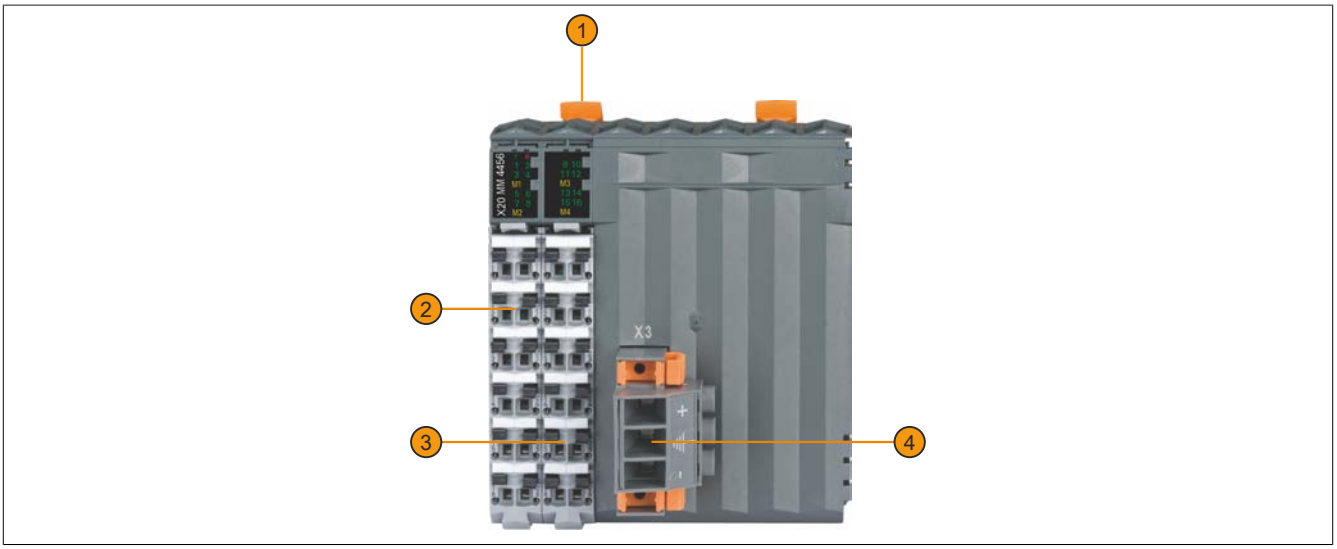
In accordance with the EN 60204-1 standard, a cable cross section of 1.5 mm² or larger must be used for the motor outputs in order to handle the maximum motor current of 10 A. To ensure full motor power, voltage drops that could result from the cable length and the electrical connections must also be taken into consideration when selecting the attachment cable.

Warning!

The terminal block is not permitted to be plugged in or unplugged during operation.

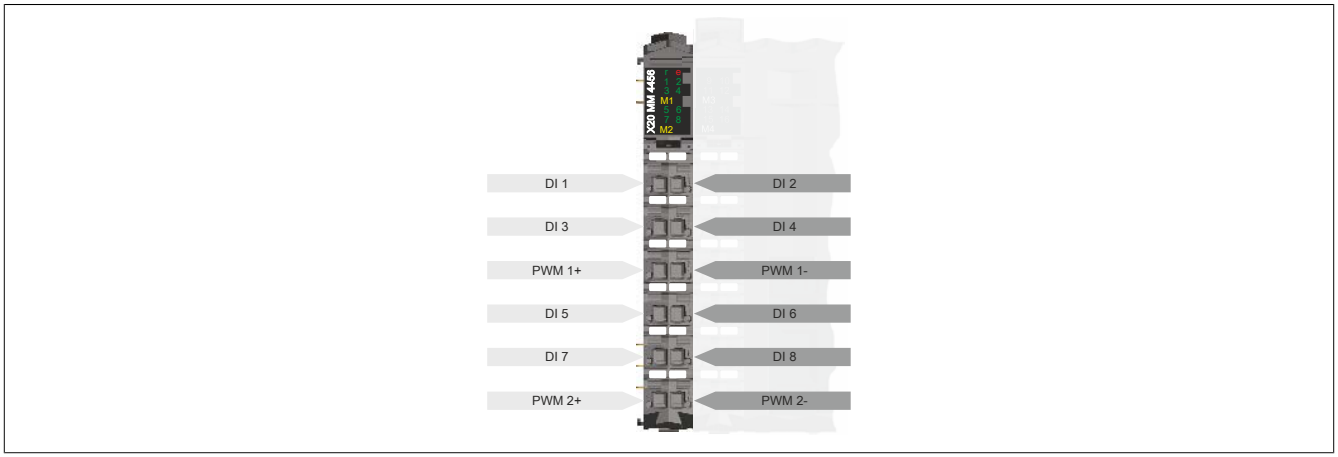
Information:

Shielded motor cables must be used in order to meet the limits according to the EN 55011 standard (emissions).

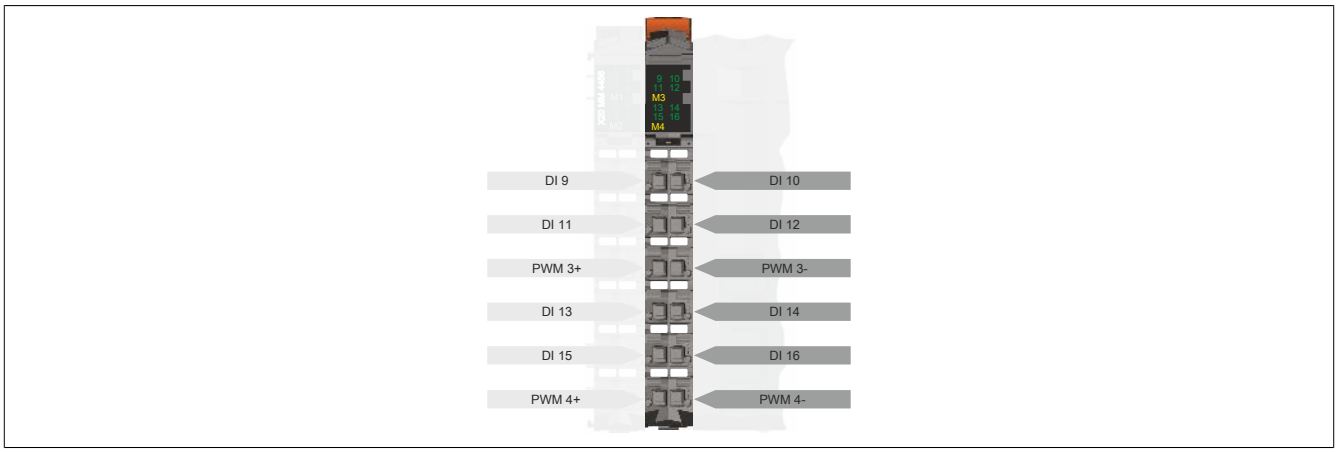


1	Top-hat rail latch	2	Terminal block X1: DI 1 - 8 / PWM 1 + 2
3	Terminal block X2: DI 9 - 16 / PWM 3 + 4	4	Terminal block X3: Module supply

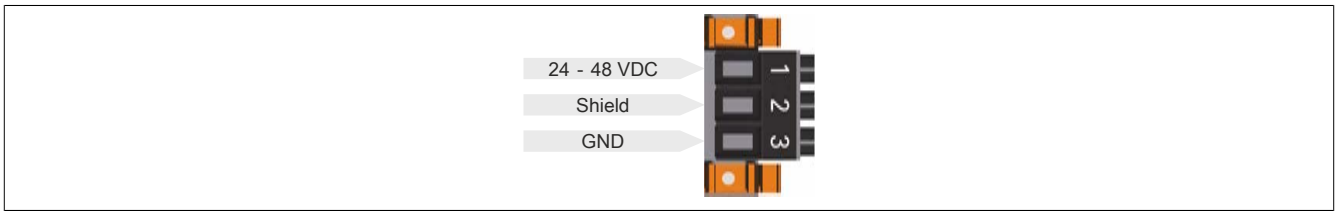
5.1 Terminal block X1 - DI 1 - 8 / PWM 1 + 2



5.2 Terminal block X2 - DI 9 - 16 / PWM 3 + 4



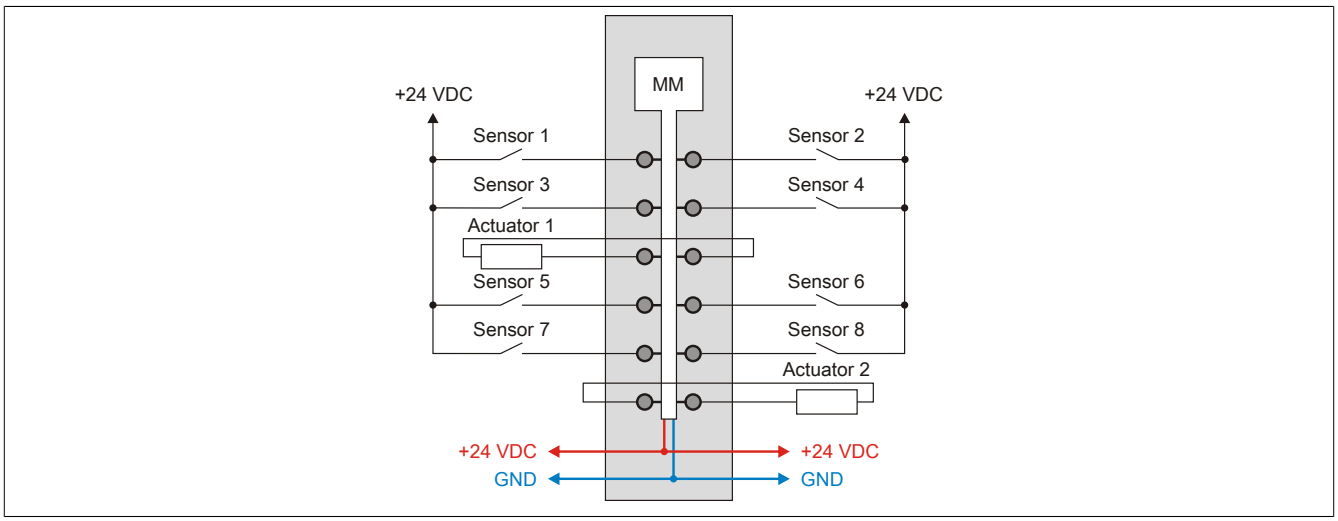
5.3 X3 terminal block - Module supply



6 Connection examples

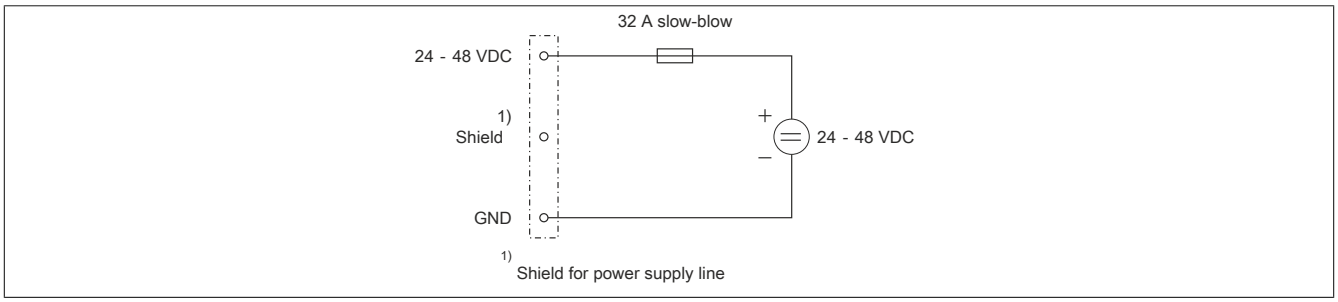
X1 and X2 terminal blocks

The following image shows a connection example for the X1 terminal block. The connection example also applies to the X2 terminal block.



X3 terminal block

For information on the fuse used, see "Protection" on page 8.



7 Possible uses for digital inputs

Digital input channels 1 to 16 can be used as follows:

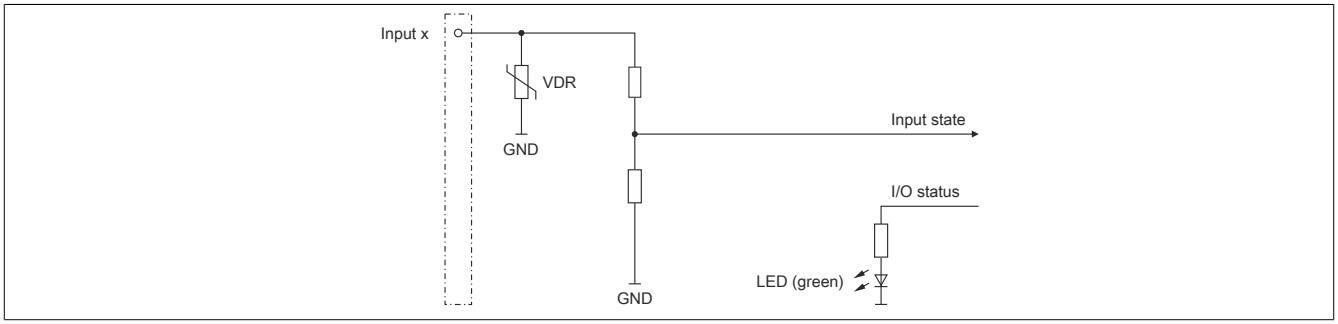
Channel	Function	Special functions
DI 1	Digital input	A
DI 2	Digital input	B
DI 3	Digital input	Limit switch, trigger, reference pulse
DI 4	Digital input	Limit switch, trigger, reference enable
DI 5	Digital input	A
DI 6	Digital input	B
DI 7	Digital input	Limit switch, trigger, reference pulse
DI 8	Digital input	Limit switch, trigger, reference enable
DI 9	Digital input	A
DI 10	Digital input	B
DI 11	Digital input	Limit switch, trigger, reference pulse
DI 12	Digital input	Limit switch, trigger, reference enable
DI 13	Digital input	A
DI 14	Digital input	B
DI 15	Digital input	Limit switch, trigger, reference pulse
DI 16	Digital input	Limit switch, trigger, reference enable

The functions can also be mixed:

Example 1	
Channel	**Function**
DI 1	Digital input
DI 2	Digital input
DI 3	Digital input
DI 4	Digital input
DI 5	Digital input
DI 6	Digital input
DI 7	Digital input
DI 8	Digital input
DI 9	A
DI 10	B
DI 11	R
DI 12	
DI 13	A
DI 14	B
DI 15	R
DI 16	

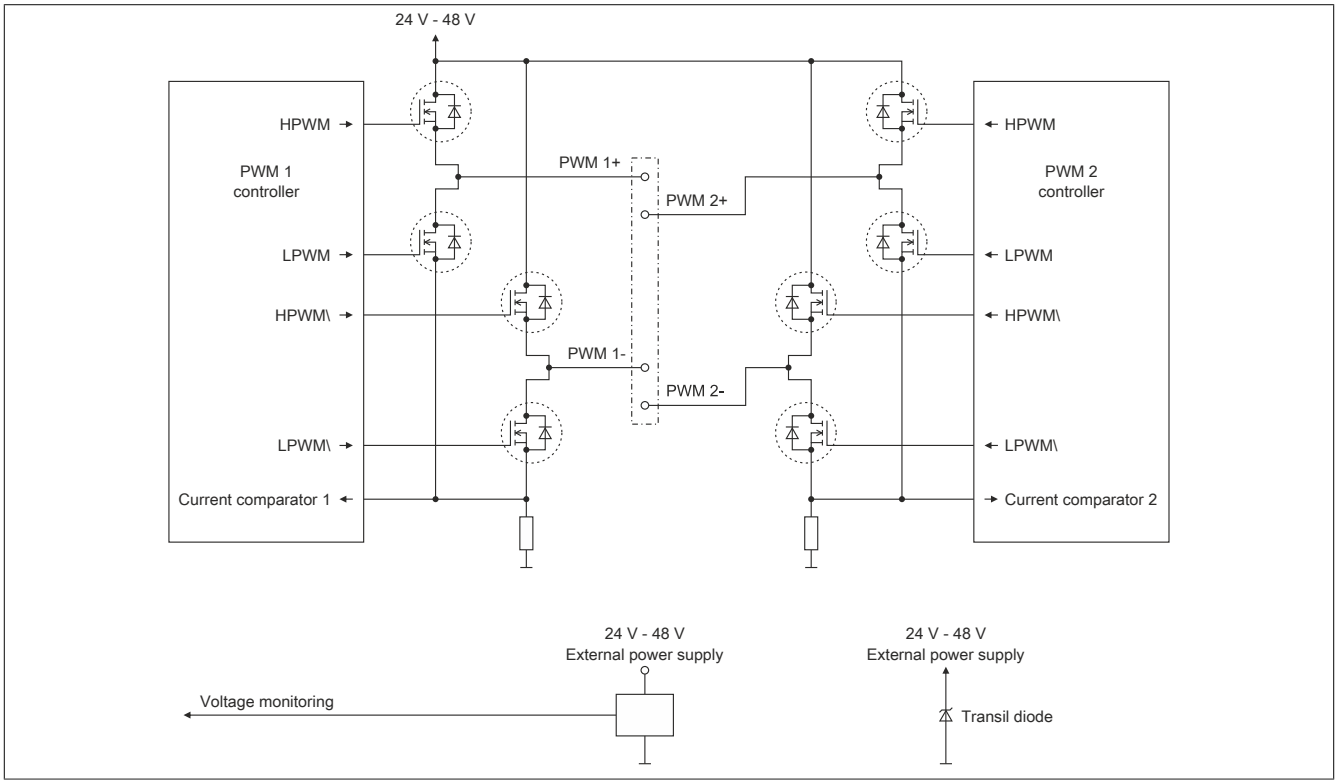
Example 2	
Channel	**Function**
DI 1	A
DI 2	B
DI 3	R
DI 4	
DI 5	Digital input
DI 6	Digital input
DI 7	Digital input
DI 8	Digital input
DI 8	Digital input
DI 10	Digital input
DI 11	Digital input
DI 12	Digital input
DI 13	A
DI 14	B
DI 15	R
DI 16	

8 Input circuit diagram



9 Output circuit diagram

The following image shows the output circuit diagram for the outputs 1 and 2. The diagram also applies to the outputs 3 and 4.



10 Protection

The power supply line should be protected by a circuit breaker or a fuse. In general, dimensioning the supply line and overcurrent protection depends on the structure of the power supply (modules can be connected individually or in groups).

Information:

The effective current for the power supply depends on the load, but is always less than the sum of the output currents. Make sure that the maximum nominal current of 31 A per pin is not exceeded on the power supply terminals of the power unit.

When choosing a suitable fuse, the user must also account for characteristics such as aging effects, temperature derating, overcurrent capacity and the definition of the rated current, which can vary by manufacturer and type. In addition, the fuse that is selected must also be able to handle application-specific characteristics (e.g. overcurrent that occurs in acceleration cycles).

The cross section of the power mains and the rated current of the overcurrent protection used are chosen according to the current load so that the maximum current load for the cable cross section selected (based on the type of layout, see table) is greater than or equal to the current load in the power mains. The rated current of the overcurrent protection must be less than or equal to the maximum current load for the cable cross section selected (based on the type of layout, see table):

$$I_{Mains} \leq I_b \leq I_Z$$

Mains ≤ Fuse ≤ Line/cable

Wire cross section [mm²]	Current load of the cable cross section I_Z / rated current of the over current protection I_b [A] according to type of installation in an ambient air temperature of 40°C in accordance to EN 60204-1			
	B1	**B2**	**C**	**E**
1.5	13.5 / 13	13.1 / 10	15.2 / 13	16.1 / 16
2.5	18.3 / 16	16.5 / 16	21 / 20	22 / 20
4	24 / 24	23 / 20	28 / 25	30 / 25
6	32 / 32	29 / 25	36 / 32	37 / 32

Table 3: Cable cross section of the mains supply line depending on the type of layout

The tripping current of the fuse cannot exceed the rated current of fuse I_b.

Type of layout	Description
B1	Wires in conduit or cable duct
B2	Cables in conduit or cable duct
C	Cables or wires on walls
E	Cables or wires on open cable tray

Table 4: Type of layout for the mains supply line

11 Monitoring the module supply

The module supply is continually monitored. If the following limits are exceeded in either direction, an error bit is set.

Upper limit:	>80 V
Warning stage:	>60 V
Lower limit:	<18 V

12 Overvoltage cutoff

If the supply voltage on the module exceeds 80V (e.g. through feedback during generator operation), then all PWM outputs are disabled (PWM output pins are short-circuited). The outputs are reactivated as soon as the supply voltage is back in the valid range. Switching the outputs on again can cause an open load error in current mode (depending on the current setpoint and load inductance) as well as with any other abrupt change to the current setpoint value.

13 Overtemperature cutoff (at 85°C)

If the module temperature reaches or exceeds the limit value of 85°C, then the module executes the following actions:

- Setting the "overtemperature" error bit
- The PWM outputs are disabled (short-circuited)

Once the module temperature sinks to 83°C, the error bit is automatically cleared by the module and the outputs become operational again.

14 Measurement of effective current

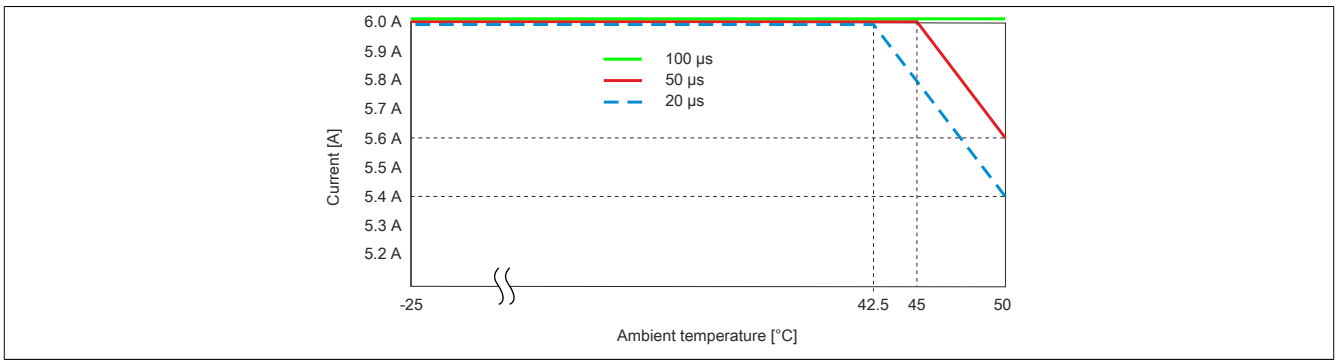
In current controller mode (see bit 12 in the "configuration register" on page 13), there is an apparent deviation between the current setpoint and the measured effective current.

This is due to how the module operates. The PWM output remains "On" or in "Fast Decay" as long as needed to reach the current setpoint. Therefore, the current setpoint is the maximum or minimum current in a specified PWM cycle. This is why the effective current of this cycle (average current of this cycle) is lower (PWM = "On") or higher (PWM = "Fast Decay") than the current setpoint.

The size of the deviation depends on the load impedance.

15 Derating

The temperature of the module is affected by the PWM period duration. The following derating must therefore be taken into account with a PWM period duration under 100 µs.



16 Let-through current I2T

The module is designed for let-through current of 360 A²s for a period of 10 seconds. If more current is needed for a certain time, less current must be drawn during the remaining time in order to maintain the let-through current.

Calculating the remaining-time current

$$I_{Boost}^{2} * t_{Boost} + I_{Remaining}^{2} * \left(10 - t_{Boost}\right) \leq 360A^2s$$

$$I_{Remaining} = \sqrt{\frac{360A^2 s - I_{Boost}^{2} * t_{Boost}}{10s - t_{Boost}}}$$

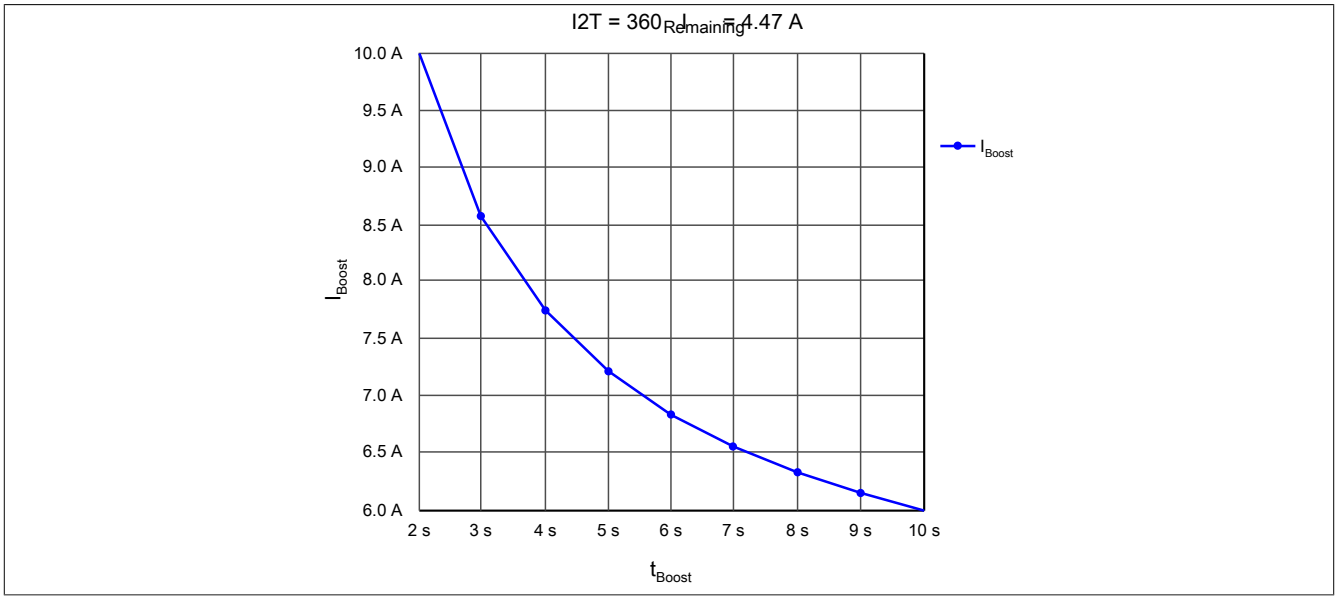
Example

A boost current of 8 A is needed for a duration of 3 seconds.

$$I_{Remaining} = \sqrt{\frac{360A^2 s - 8A^2 * 3s}{10s - 3s}} = 4.89A$$

t_{Boost}	I_{Boost}	$t_{Remaining}$	$I_{Remaining}$	I2T
s	A	s	A	A² * s
10	6.00	0	0	360.00
2	10.00	8	4.47	360.00
3	8.57	7	4.47	360.00
4	7.75	6	4.47	360.00
5	7.21	5	4.47	360.00
6	6.83	4	4.47	360.00
7	6.55	3	4.47	360.00
8	6.32	2	4.47	360.00
9	6.15	1	4.47	360.00

These values correspond to the following curve for let-through current I2T:



17 Register description

17.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" in the X20 system user's manual.

17.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration						
64	ConfigOutput01	USINT				•
65	ConfigOutput02	USINT				•
72 + (N-1) * 8	Configuration0N (index N = 1 to 4)	UINT				•
74 + (N-1) * 8	HoldingCurrent0N (index N = 1 to 4)[1)]	INT				•
76 + (N-1) * 8	BoostCurrent0N (index N = 1 to 4)[1)]	INT				•
78 + (N-1) * 8	BoostTime0N (index N = 1 to 4)[1)]	UINT				•
104 + (N-1) * 2	SwitchingPeriod0N (index N = 1 to 4)[1)]	UINT				•
Communication						
0 + (N-1) * 8	PulseWidthCurrentPWM0N (index N = 1 to 4)	INT			•	
0 + (N-1) * 8	Counter0N (index N = 1 to 4)	INT	•			
2 + (N-1) * 8	CounterLatch0N (index N = 1 to 4)	INT	•			
2 + (N-1) * 8	Control	USINT			•	
	TriggerEdge0N	Bit 0				
	StartTrigger0N	Bit 1				
	StartLatch0N	Bit 2				
	DitherDisable0N	Bit 3				
	ClearError0N	Bit 4				
	ShowMeanCurrent0N	Bit 5				
	ResetCounter0N	Bit 6				
	OutputEnable0N	Bit 7				
4	PeriodDurationPWM	UINT			•	
4 + (N-1) * 8	usSinceTrigger0N (index N = 1 to 4)	UINT	•			
6 + (N-1) * 8	Status0N (index N = 1 to 4)	USINT	•			
	StatusInput(N-1)*4 + 1	Bit 0				
	...	...				
	StatusInput(N-1)*4 + 4	Bit 3				
	nLatchPending0N	Bit 4				
	LatchDone0N	Bit 5				
	EndswitchReached0N	Bit 6				
	PWMError0N	Bit 7				
7	Global error	USINT	•			
	OverVoltageError	Bit 4				
	UnderVoltageError	Bit 5				
	VoltageWarning	Bit 6				
	OvertemperatureError	Bit 7				
15	Channel errors	USINT	•			
	CurrentError01	Bit 0				
	OverCurrentError01	Bit 1				
	CurrentError02	Bit 2				
	OverCurrentError02	Bit 3				
	CurrentError03	Bit 4				
	OverCurrentError03	Bit 5				
	CurrentError04	Bit 6				
	OverCurrentError04	Bit 7				
128	ModuleTemperature	SINT		•		

1) Only available with firmware version 102 or later

17.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration							
64	-	ConfigOutput01	USINT				•
65	-	ConfigOutput02	USINT				•
72 + (N-1) * 8	-	Configuration0N (index N = 1 to 4)	UINT				•
74 + (N-1) * 8	-	HoldingCurrent0N (index N = 1 to 4)	INT				•
76 + (N-1) * 8	-	BoostCurrent0N (index N = 1 to 4)	INT				•
78 + (N-1) * 8	-	BoostTime0N (index N = 1 to 4)	UINT				•
104 + (N-1) * 2	-	SwitchingPeriod0N (index N = 1 to 4)	UINT				•
Communication							
0 + (N-1) * 8	0 + (N-1) * 8	PulseWidthCurrentPWM0N (index N = 1 to 4)	INT			•	
0 + (N-1) * 8	0 + (N-1) * 8	Counter0N (index N = 1 to 4)	INT	•			
2 + (N-1) * 8	2 + (N-1) * 8	CounterLatch0N (index N = 1 to 4)	INT	•			
2 + (N-1) * 8	2 + (N-1) * 8	Control	USINT			•	
		TriggerEdge0N	Bit 0				
		StartTrigger0N	Bit 1				
		StartLatch0N	Bit 2				
		DitherDisable0N	Bit 3				
		ClearError0N	Bit 4				
		ShowMeanCurrent0N	Bit 5				
		ResetCounter0N	Bit 6				
		OutputEnable0N	Bit 7				
4	4	PeriodDurationPWM	UINT			•	
4 + (N-1) * 8	4 + (N-1) * 8	usSinceTrigger0N (index N = 1 to 4)	UINT	•			
6 (N-1) * 8	6 (N-1) * 8	Status of the inputs	U(S)INT	•			
		StatusInput(N-1) * 4 + 1	Bit 0				
		...	...				
		StatusInput(N-1) * 4 + 4	Bit 3				
		nLatchPending0N	Bit 4				
		LatchDone0N	Bit 5				
		EndswitchReached0N	Bit 6				
		PWMError0N	Bit 7				
		CurrentError01	Bit 8				
		OverCurrentError01	Bit 9				
		CurrentError02	Bit 10				
		OverCurrentError02	Bit 11				
		CurrentError03 OverVoltageError	Bit 12				
		OverCurrentError03 UnderVoltageError	Bit 13				
		CurrentError04 VoltageWarning	Bit 14				
		OverCurrentError04 OvertemperatureError	Bit 15				
128	-	ModuleTemperature	SINT		•		

1) The offset specifies the position of the register within the CAN object.

17.3.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use other registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" in the X20 user's manual (version 3.50 or later).

17.3.2 CAN I/O bus controller

The module occupies 4 analog logical slots on CAN I/O.

17.4 Configuration

17.4.1 Configuration

Name:
Configuration01 to Configuration04

These registers can be used to configure the 4 DC motors.

The following placeholders are used in the configuration table:

Register	Channel N	In1	In2
Configuration01	1	DI3	DI4
Configuration02	2	DI7	DI8
Configuration03	3	DI11	DI12
Configuration04	4	DI15	DI16

Data type	Values	Bus controller default setting
UINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0 - 1	Configuration of the latch function for ABR counter **N**. Enabling the latch function is described in the control register (bit 2):	00	ABR counter **N** is latched unconditionally (default setting). The reference enable input is ignored (bus controller default setting).
		01	ABR counter **N** is latched if a rising edge occurs on digital input **In1** and reference enable input **In2** is "1". The reference enable input must be enabled to do this (see bit 2).
		10	ABR counter **N** is latched if a falling edge occurs on digital input **In1** and reference enable input **In2** is "1". The reference enable input must be enabled to do this (see bit 2).
		11	The latch function is disabled.
2	Reference enable input:	0	No reference enable input (bus controller default setting)
		1	Digital input **In2** is used as the reference enable input.
3	Active level of the reference enable input for ABR counter **N**:	0	Active level = High (bus controller default setting)
		1	Active level = Low
4	Reserved	0	
5 - 7	Definition of the limit switch **N** (see also "Limit switch function" on page 14):	000	Limit switch **N** is disabled (bus controller default setting)
		001	Digital input **In1** is used as the Enable input.[1)]
		010	Digital input **In1** is used as the limit switch.
		011	Reserved
		100	Digital input **In2** is used as the limit switch.
		101	Reserved
		110	Digital inputs **In1** and **In2** are used as the left and right limit switches.
		111	Reserved
8	Active level for limit switch **N**:	0	Active level = High (bus controller default setting)
		1	Active level = Low
9 - 10	Trigger input for trigger counter "usSinceTrigger" **N**:	00	The trigger counter is disabled (bus controller default setting).
		01	Digital input **In1** is used as the trigger input.
		10	Digital input **In2** is used as the trigger input.
		11	Reserved
11	Display of current average for output **N**:	0	If the corresponding setting has been enabled, then the average current value is indicated in register "CounterLatch[x]" on page 20 (see bit 5 in the "control register" on page 14) (bus controller default setting)
		1	If the corresponding setting has been enabled, then the average current value is indicated in register "usSinceTrigger[x]" on page 21 (see bit 5 in the "control register" on page 14).
12 + 15	Output mode **N**:	00	PWM mode (bus controller default setting)
		01	Current mode
		10	Boost-and-hold current control[1)]
		11	Reserved
13 - 14	Decay configuration for PWM **N** (see also "Decay configuration" on page 24):	00	Slow decay (bus controller default setting)
		01	Mixed decay
		10 - 11	Reserved

1) Only available with firmware version 102 or later

Limit switch function

The limit switch function serves to quickly shut off the PWM outputs when a limit position is reached.

The limit switch is activated and the disable edge (rising or falling) on the limit switch input is selected using bits 6 to 8.

A PWM output is disabled as soon as the configured disable edge is reached on the corresponding input of the limit switch. This cutoff occurs independently of the current direction of movement. It remains disabled until either the limit switch function is disabled or the limit switch is acknowledged with bit 4 in the corresponding "control register" on page 14.

Enable input

The limit switch input of the module can optionally be used as an enable input. Bits 5 to 7 must be configured accordingly for this. Data point OutputEnable and the digital input are logically linked by an AND operator.

When the enable input is enabled, the PWM output can be switched on and off via the digital input. Switching on and off is done with a jitter of 50 µs. Since it is possible to react only at the beginning of the PWM period, an additional jitter of the length of the PWM period duration must be taken into account.

17.4.2 Control

Name:
TriggerEdge01 to TriggerEdge04
StartTrigger01 to StartTrigger04
StartLatch01 to StartLatch04
DitherDisable01 to DitherDisable04
ClearError01 to ClearError04
ShowMeanCurrent01 to ShowMeanCurrent04
ResetCounter01 to ResetCounter04
OutputEnable01 to OutputEnable04

These registers can be used to configure the behavior of the trigger, the ABR counter and the dither.

[N] stands for the index number of the register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	TriggerEdge**N** Configuration of trigger edge for "usSinceTrigger":	0	Counting starts at rising edge
		1	Counting starts at falling edge
1	StartTrigger**N** Enabling of "usSinceTrigger" due to a status change of bit 1	x	Counting starts at the next trigger edge (see bit 0). For more information about trigger functionality, see "Trigger function procedure" on page 15.
2	StartLatch**N** Latching or referencing ABR counters:	0	Disabled
		1	Enabled
3	DitherDisable **N**	0	Dither for PWM output **N** is switched on. The dither frequency and dither amplitude must be greater than 0 (see "Dither" on page 18).
		1	Dither for PWM output **N** is switched off.
4	ClearError**N** Acknowledging error or limit switch:	0	No effect
		1	Error acknowledgment on output **N** (overcurrent or open load) or acknowledgment of limit switch **N**
5	ShowMeanCurrent**N** Konfiguration der Register "CounterLatch" on page 20 und "usSinceTrigger" on page 21	0	Register CounterLatch**N** contains the latched counter value. Register usSinceTrigger**N** contains the trigger counter.
		1	Both registers contain the current PWM output current
6	ResetCounter**N** Reset ABR counter	0	Enable ABR counter
		1	Reset ABR counter
7	OutputEnable**N**[1]	0	Switch off the PWM output
		1	Switch on the PWM output

1) Only for boost-and-hold current control.

Trigger function procedure

The following points must be taken into consideration when configuring or activating the trigger function:

- Select the desired trigger edge using bit 0
- Enable the trigger function by changing the state of StartTrigger (bit 1). This edge clears the register usSinceTrigger (µs counter).
- When the trigger event occurs, the µs counter "usSinceTrigger" is started
- The "usSinceTrigger" counter cannot overrun, i.e. the counter is stopped at 2^{16}-1 and retains this value until the next time the trigger function is activated
- The trigger function can be re-activated at any time by changing the state of StartTrigger (bit 1) regardless of if a trigger event has occurred or if "usSinceTrigger" has reached its maximum value.

Reset ABR counter

Bit 6 sets the following counters and status bits to 0:

- ABR counter
- Latch value of the ABR counter
- Latching started on the ABR counter (bit 4 of the "status register" on page 22)
- ABR counter successfully latched (bit 5 of the "status register" on page 22)

Please note that a started latch procedure is no longer active after the ABR counter has been reset. This means that latching must be restarted by a rising edge on bit 2.

OutputEnable

Bit 7 can start or stop the output profile in Boost-and-hold current control. If a rising edge occurs on this data point, any pending Overcurrent error or Open load error of the associated PWM output are acknowledged and the output is switched on.

Starting or stopping occurs immediately after the transfer of the value on the X2X Link network with a jitter of 50 µs. Note that during startup, an additional jitter of the length of the PWM period duration of the current controller is added.

Starting and stopping the output profile can also be controlled by the digital input. See "Enable input" on page 14.

17.4.3 Difference between operating modes

The module provides the following operating modes:

- PWM mode
- Current mode
- Boost-and-hold current control

The following graphics show how the voltage or current curve of the outputs is affected by registers "PWM period duration" on page 20 and "PWM pulse width" on page 20.

PWM mode

At the beginning of each period, the output is switched on for the percentage of time set in the PWM pulse width.

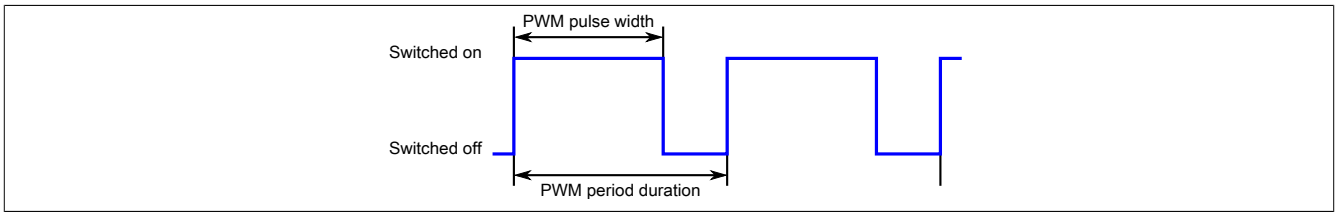


Figure 1: Voltage curve during PWM mode

Current mode

At the beginning of each period, the current output is switched on. After reaching the value set in "PulseWidthCurrentPWM" on page 20, the output is switched off and the voltage drops according to the set decay configuration until it is next switched on.

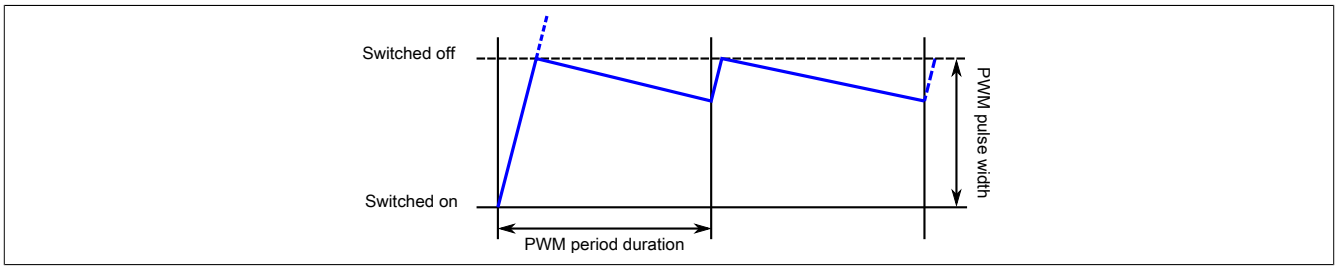


Figure 2: Current curve during current mode

Boost-and-hold current control

Information:

Only available with firmware version 102 or later.

In this operating mode, the current mode is combined with a higher-level PWM mode.

After the time (t_{Boost}) set in register "BoostTime" on page 17, the inrush current (I_{Boost}) is changed to the holding current ($I_{Holding}$) specified in register "HoldingCurrent" on page 17.

The period duration of the current profile is set in register "SwitchingPeriod" on page 17 in 50-µs steps. In addition, the PWM period duration must be set in register PeriodDurationPWM. (Not shown, see Current mode.)

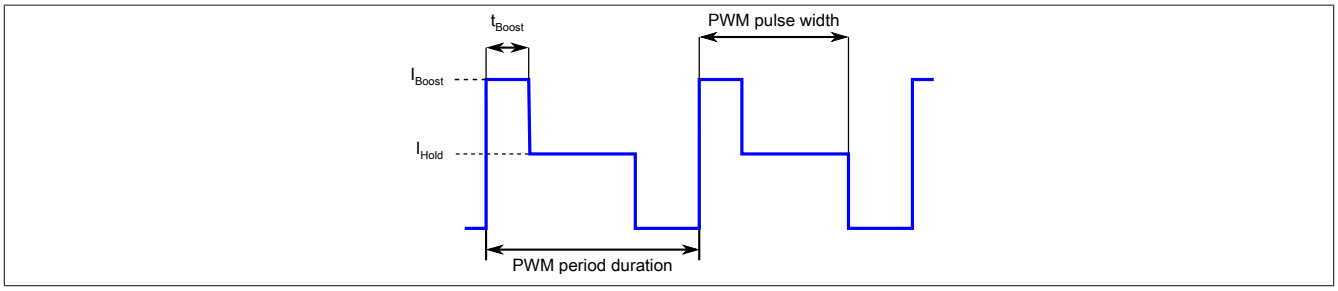


Figure 3: Current curve during boost-and-hold mode

17.4.3.1 Example: Controlling a digital valve

The boost current (I_{Boost}) is used to quickly open a digital valve, for example. After the boost time (t_{Boost}), the current is reduced to the lower holding current ($I_{Holding}$) in order to save energy and not overload the PWM output. $I_{Holding}$ is therefore set to a smaller value than I_{Boost}.

The pulse width can be used to set the opening time of the valve in relation to the period duration. After the period duration has expired, I_{Boost} is started again. If the valve should remain open continuously, the pulse width must be set to 100%. In this case, no boost current is output at the beginning of the next period.

I_{Boost} is only output if the valve has been switched off for at least 50 µs. If the pulse width is set smaller than t_{Boost}, the boost time is shortened accordingly.

17.4.4 Boost-and-hold registers

17.4.4.1 Boost current

Name:
BoostCurrent01 to BoostCurrent04

The boost current is set in mA in this register.

Data type	Values	Information
INT	0 to 10000	For 0 to 10 A

17.4.4.2 Boost time

Name:
BoostTime01 to BoostTime04

The sampling time is set in µs in this register. The entered value is rounded up to the next largest 50-µs interval.

Data type	Values	Information
UINT	0 to 65500	In µs

17.4.4.3 Holding current

Name:
HoldingCurrent01 to HoldingCurrent04

The holding current is set in mA in this register. After the boost time, the current for the remaining pulse width time is raised or lowered to this value.

Data type	Values	Information
INT	0 to 6000	For 0 to 6 A

17.4.4.4 Period duration of the current profile

Name:
SwitchingPeriod01 to SwitchingPeriod04

This register is used to set the period duration of the current profile in µs for boost-and-hold mode. The entered value is rounded up to the next largest 50-µs interval.

Data type	Values	Information
UINT	2000 to 65500	Corresponds to 500 to 15.26 Hz

17.4.4.5 Synchronous operation of channels

In order for 2 or more channels to run synchronously, their period durations of the output profile (SwitchingPeriod) must be set to the same value or to a multiple of the other channel. An exact phase position of 0 degrees can only be guaranteed if the channels are switched on simultaneously (in the same bus cycle) with OutputEnable.

To operate the current profile synchronously to the X2X Link network, SwitchingPeriod should be set to a multiple of the bus cycle.

17.4.5 Dither

When the position setpoint for valves remains constant for a long period of time, especially in fluids, there is a risk that a valve will stick. This is normally prevented using "dithering". When doing so, the value is permitted to slightly oscillate around the position setpoint.

By default, the dither is active for both outputs as soon as the dither amplitude and dither frequency are set to a value >0. If necessary, the dither can be disabled for each output individually or simultaneously (see bit 3 in register "control register" on page 14).

No dither is used in boost-and-hold mode of the PWM output. Any set dither amplitude and dither frequency are ignored by the module.

17.4.5.1 Dither amplitude

Name:
ConfigOutput01

This register can be used to configure the amplitude value or pulse width.

Data type	Value	Information
USINT	0 to 255	Current mode: 0 to 25.5% of the module's nominal current[1)] PWM mode: 0 to 25.5% of the period duration. Bus controller default setting: 0

1) See the technical data for the module.

17.4.5.2 Dither frequency

Name:
ConfigOutput02

This register can be used to set the frequency in 2 Hz steps.

Data type	Value	Information
USINT	0 to 255	Corresponds to 0 to 510 Hz. Bus controller default setting: 0

17.4.5.3 Dither example

The values specified in the data sheet for a valve should be used to calculate Dither amplitude and Dither frequency.

Data sheet for the valve

The data sheet for a valve manufacturer recommends the following dithering:

Dither height in percent (A_{Dither}): 20 to 35% (peak values) of the nominal valve current of 2 A

Dither frequency in Hertz (F_{Dither}): 40 to 70 Hz

Selected values

These values correspond to the average values on the valve data sheet.

A_{Dither} = 27% of the valve's nominal current (peak values)

F_{Dither} = 56 Hz

Formulas

Dither amplitude = (A_{Dither} / 2) * (Nominal current $_{Valve}$ / Nominal current$_{Module}$) * 10
Info: (A_{Dither} / 2) = Conversion of the peak values to amplitude, " * 10" = Scaling of the dither amplitude to 1/10%

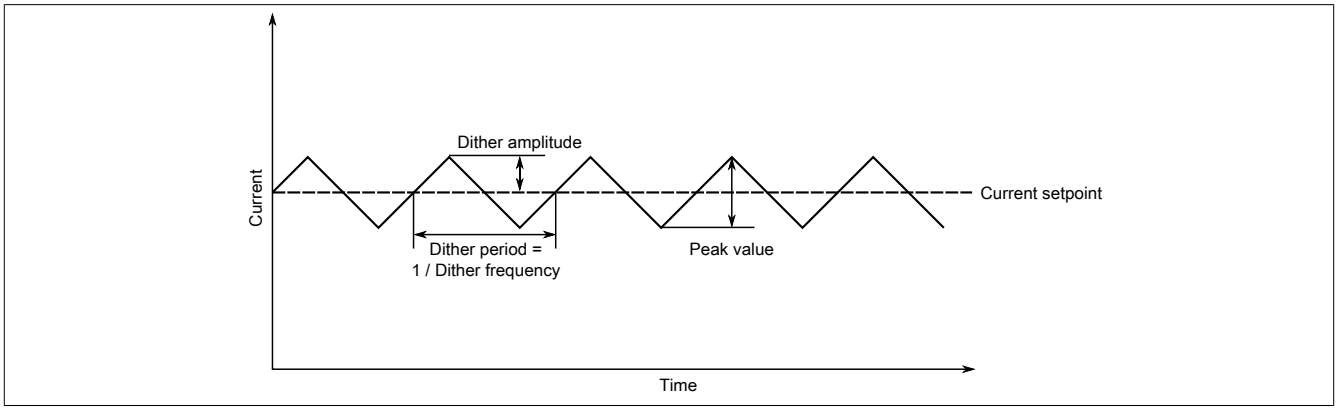
Dither frequency = F_{Dither} / 2 Hz
Info: Dither frequency is configured in 2 Hz steps.

Calculation

By using the selected values in the formulas.

Dither amplitude = 27% / 2 * (2 A / 6 A) * 10 = 45

Dither frequency = 56 Hz / 2 Hz = 28



17.5 Communication

17.5.1 PWM pulse width

Name:
PulseWidthCurrentPWM01 to PulseWidthCurrentPWM04

The PWM pulse width (PWM mode) or current setting (in current mode) is specified in this register according to the setting in the module configuration register (see also "Difference between operating modes" on page 16). A negative value changes the output polarity.

PWM mode

Data type	Value	Output +	Output -
INT	32767	High	Low
	16384	PWM 50/50	Low
	0	Low (bus controller default setting)	Low (bus controller default setting)
	-16384	Low	PWM 50/50
	-32767	Low	High

Current mode

Data type	Value	Current mode
INT	19661 to 32767	6 to 10 A (max. 2 s)
	19660	6 A
	0	0 A
	-19660	-6 A
	-19661 to -32767	-6 to -10 A (max. 2 s)

Boost-and-hold current control

In this operating mode, this register is used to control the pulse width of the output signal in a way similar to PWM mode. In contrast, the pulse width of the current profile is specified. See "Current mode" on page 16.

In this operating mode, the pulse width can be set with a resolution of 50 µs. The pulse width of the current is specified as a percentage of the period duration of output signal SwitchingPeriod. If the value of this register is modified during a period, the pulse width is immediately adjusted.

Negative values correspond to an output with negative current direction.

Data type	Values	Information
INT	-32768 to 32767	For -100% to 100%

17.5.2 PWM period duration

Name:
PeriodDurationPWM

Data type	Value	Information
UINT	20 to 65535	Time in µs

17.5.3 ABR counter

Name:
Counter01 to Counter04

These registers are 16-bit AB(R) counters.

Data type	Values
INT	-32768 to 32767

17.5.4 ABR counter latch

Name:
CounterLatch01 to CounterLatch04

When a latch event occurs, the current counter values are saved in these registers. For additional features, see bit 5 in the respective "control register" on page 14.

Data type	Values
INT	-32768 to 32767

17.5.5 Microseconds since trigger

Name:
usSinceTrigger01 to usSinceTrigger04

This register shows either the time in µs since the last trigger event or the average current value.

Counting mode

The register cannot overflow in counting mode. The data type is unsigned integer (UINT). The counter is stopped at 2^{16}-1 and retains this value until the trigger function is next enabled.

Data type	Values
UINT	0 to 65,535

Measurement of average current value

Displaying the average current value is enabled by setting bit 11 in register "Configuration0x" on page 13. The data type is integer (INT). Negative currents are indicated by values between 32769 and 65535.

Data type	Value	Information
INT	19,661 to 32,767	6 to 10 A
	19,660	6 A
	1	305 µA (= 10 A / 32,767)
	0	0 A
	65,535	-305 µA (= -10 A / 32,767)
	45,876	-6 A
	45,875 to 32,769	-6 to -10 A

17.5.6 Status of the inputs

Name:
StatusInput01 to StatusInput16
nLatchPending01 to nLatchPending04
LatchDone01 to LatchDone04
EndswitchReached01 to EndswitchReached04
PWMError01 to PWMError04

These registers contain the status of the inputs and outputs for each DC motor.

The following placeholders are used in the status table.

Register	Channel [N]	In1	In2	In3	In4
Status of inputs 1	1	DI1	DI2	DI3	DI4
Status of inputs 2	2	DI5	DI6	DI7	DI8
Status of inputs 3	3	DI9	DI10	DI11	DI12
Status of inputs 4	4	DI13	DI14	DI15	DI16

Data type	Values
USINT[1)]	See the bit structure.
UINT[2)]	See the bit structure.

1) Function model 0 and function model 254 → Registers "Status of inputs 3" and "Status of inputs 4"
2) Only function model 254 → Registers "Status of inputs 1" and "Status of inputs 2"

Bit structure:

Bit	Description	Value	Information
0	StatusInput **[In1]**	x	**In1** is used with ABR counter **N** for encoder signal A.
1	StatusInput **[In2]**	x	**In2** is used with ABR counter **N** for encoder signal B.
2	StatusInput [**In3]**	0	Possible uses of the digital input • Trigger input **N** • Reference pulse for ABR counter **N** • Limit switch **N** (left)
3	StatusInput **[In4]**	0	Possible uses of the digital input • Reference enable **N** • Trigger input **N** • Limit switch **N** (right)
4	nLatchPending **[x]**	00	Latching is started.
		01	ABR counter latch **N** is ready. Latch not yet started.
5	LatchDone **[x]**	0	After each successful latch of ABR counter **N**, the status of this bit is changed.
6	EndswitchReached **[x]**	00	No effect on PWM output **N**
		01	Limit switch **N** is reached. PWM output **N** is switched off.
7	PWMError **[x]**	0	No channel error
		1	Channel error occurred. PWMError **[x]** is a summary of the two error bits CurrentError0x and OverCurrentError0x in register "Channel errors" on page 23. PWMError **[x]** is not affected by the error flags contained in the "global errors" on page 24 register. In order to intercept error states that can affect the PWM outputs, the global errors register must also be monitored.
8 - 15	**Function model 254 only**		
	Status of inputs 1	x	With "Status of inputs 1", bits 12 to 15 contain error bits 4 to 7 of register "Global error" on page 24.
	Status of inputs 2	x	With "Status of inputs 2", bits 8 to 15 contain error bits 0 to 7 of register "Channel errors" on page 23.

17.5.7 Channel errors

Name:
CurrentError01 to CurrentError04
OverCurrentError01 to OverCurrentError04

If an error is detected, the corresponding error bit in this register remains set until the error is acknowledged using bit 4 in the respective "control register" on page 14.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	CurrentError01	0	No error
		1	Open load error
1	OverCurrentError01	0	No error
		1	Overcurrent error, output deactivated.
2	CurrentError02	0	No error
		1	Open load error
3	OverCurrentError02	0	No error
		1	Overcurrent error, output deactivated.
4	CurrentError03	0	No error
		1	Open load error
5	OverCurrentError03	0	No error
		1	Overcurrent error, output deactivated.
6	CurrentError04	0	No error
		1	Open load error
7	OverCurrentError04	0	No error
		1	Overcurrent error, output deactivated.

Overcurrent error

An overcurrent error is registered if one of the following conditions is met:

- ≥10 A flow from a PWM output for at least 2 seconds
- ≥16 A flow for 3 consecutive PWM cycles
- All PWM outputs together consume more than 32 A on the X3 connector

In all three cases, the affected PWM output is deactivated by the firmware (i.e. the pins on the PWM output are short-circuited). The user must acknowledge the error using bit 4 in the respective "control register" on page 14 before a PWM output deactivated in this manner can be made operational again.

Open load error

An open load error is only registered in current control mode (see bit 12 in the respective "configuration register" on page 13) if the current setpoint is not reached. In some cases this can be caused by an open line, although usually the impedance of the load is too high.

17.5.8 Global error

Name:
OverVoltageError
UnderVoltageError
VoltageWarning
OvertemperatureError

This register indicates overtemperature and errors in the module supply. The error bits are automatically acknowledged by the module as soon as the values are back within the permissible limits.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Reserved	0	
4	OverVoltageError	0	No error
		1	Voltage >80 V. All outputs are deactivated.
5	UnderVoltageError	0	No error
		1	Voltage <18 V
6	VoltageWarning	0	No error
		1	Voltage >60 V
7	OvertemperatureError	0	No error
		1	Module overtemperature; all outputs are deactivated.

17.5.9 Temperature

Name:
ModuleTemperature

The module temperature is displayed in this register.

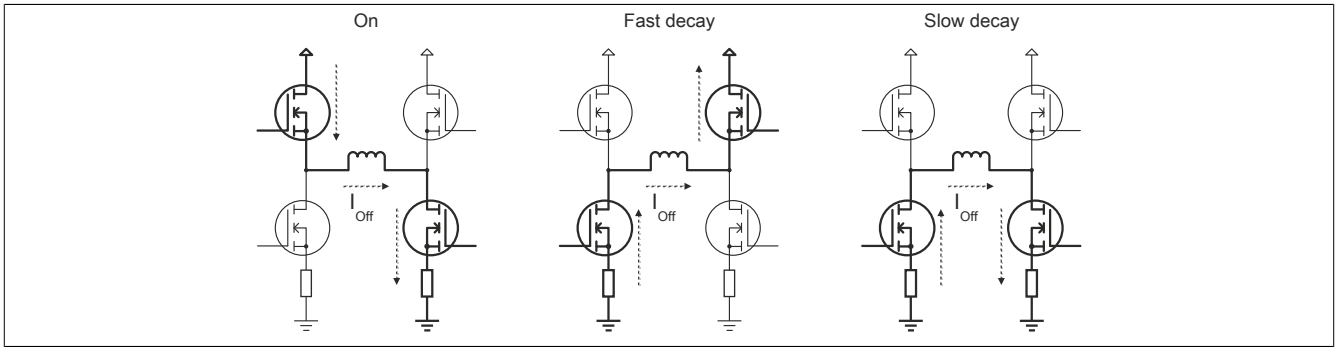
Data type	Value	Information
SINT	-40 to 125	Module temperature in °C

17.6 Decay configuration

The decay configuration determines the method and dynamics of current reduction for inductive loads or motors.

"Slow decay" is configured by default. In this mode, the current is automatically reduced relatively slowly with resistance in the load. No energy is regenerated into the module.

"Mixed decay" mode is recommended for applications that require a dynamic and linear reduction of current. In this mode, energy is regenerated into the module during part of the PWM cycle (fast decay).



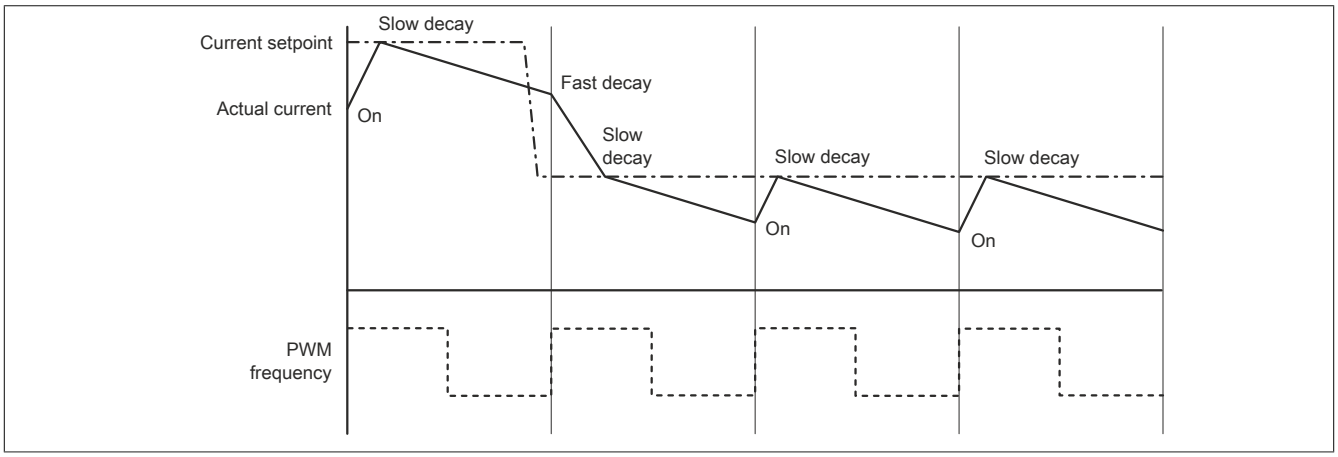
17.6.1 Current control

As its name suggests, mixed decay mode is a mix of "slow decay" and "fast decay". This occurs as follows:

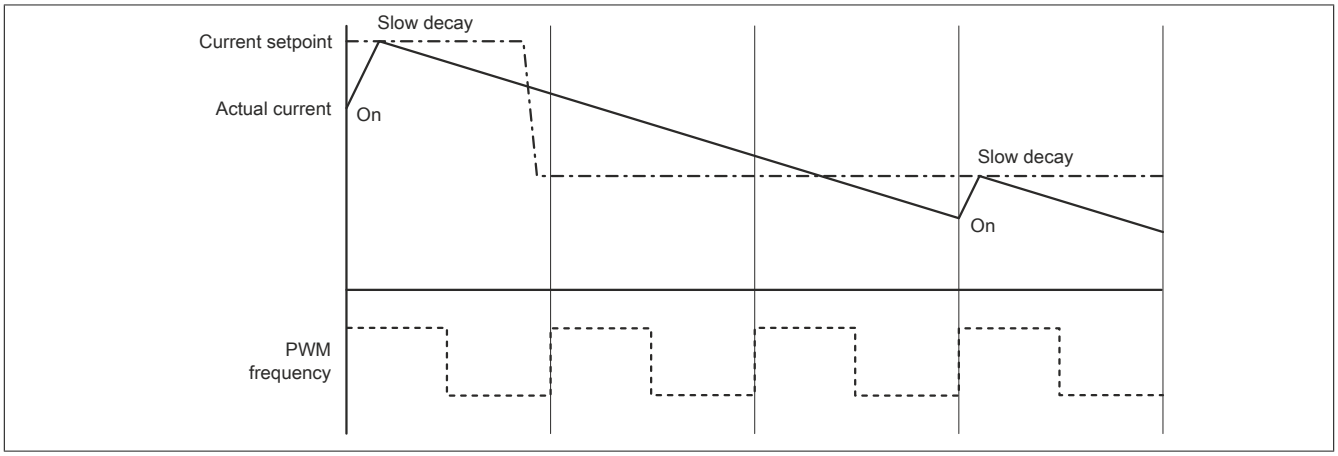
A check is made at the beginning of each PWM cycle to determine if the actual current for the phases is below the set current. If this is the case, PWM is enabled (On) until the current setpoint is reached. If the current setpoint has already been exceeded at the beginning of the PWM cycle (generator operation), the system immediately switches to fast decay mode until the current setpoint is exceeded. The rest of the PWM cycle always takes place in slow decay mode.

This also permits generator operation as long as the valid range for the supply voltage has not been exceeded due to the regeneration into the DC circuit.

Current control in Mixed Decay mode



Current control in Slow Decay mode

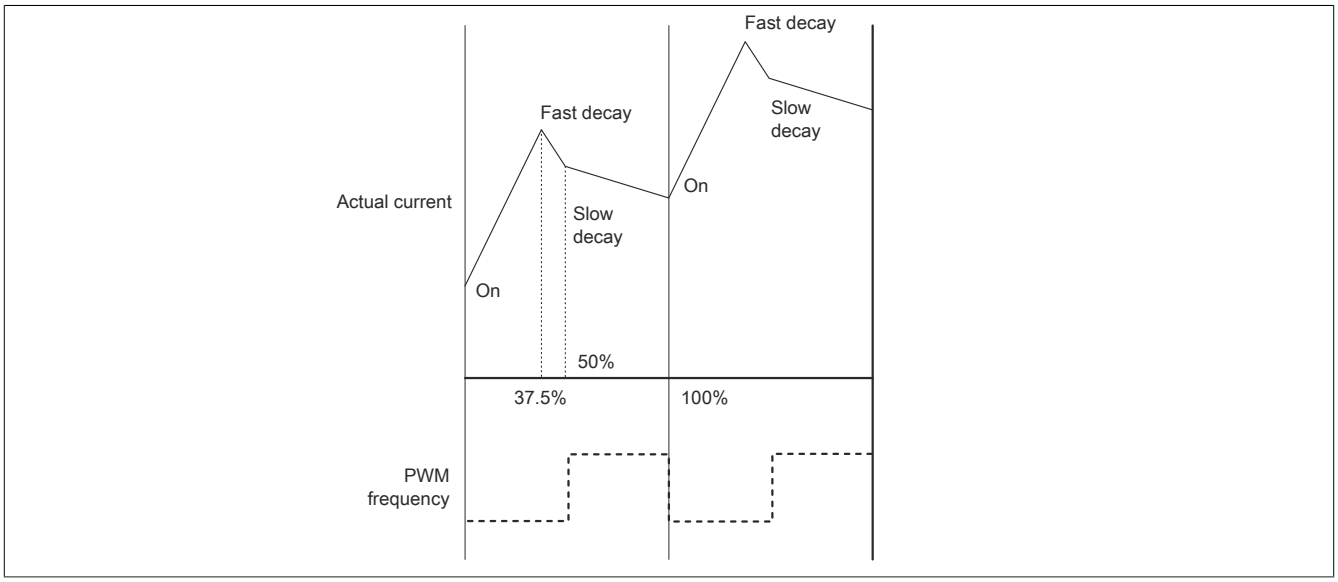


17.6.2 PWM control

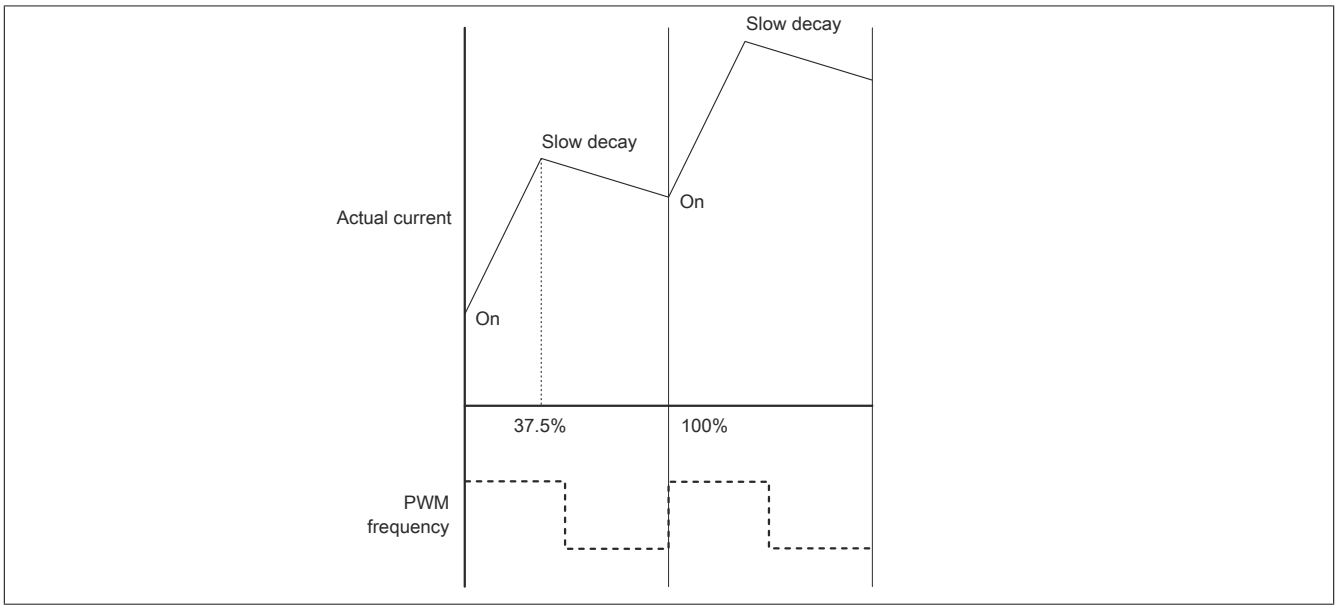
When Mixed Decay mode is enabled, the outputs are driven in Fast Decay mode up until 50% of the period and in Slow Decay mode for the remainder of the switch-off phase.

When Slow Decay mode is used, it is immediately enabled during the switch-off phase.

PWM control in Mixed Decay mode (pulse duty factor = 37.5%)



PWM control in Slow Decay mode (pulse duty factor = 37.5%)



Operating DC motors

In PWM mode, the motor current is limited to the maximum current (10 A), independent of the supply voltage.

However, the motor switches to generator operation when braking. Because of the counter EMF, which is dependent on the rotary speed, a current is generated in the module that is only limited by the internal resistance of the motor. This is not permitted to exceed 15 A (maximum 2 seconds).

The counter EMF closely corresponds to the voltage needed to achieve this speed. Therefore, the maximum brake current is very easy to calculate with the following formula.

$$I_{Brake} = U_e * \frac{PulseWidth}{100\%} * \frac{1}{R_{Motor}}$$

Example:

Module supply	42 V
Pulse width	16364 (equal to 50%)
Internal resistance of motor	3.5 Ω

$$I_{Brake} = 38\ V * \frac{50}{100\%} * \frac{1}{3.5\Omega} = 5.4A$$

17.7 Minimum cycle time

The minimum cycle time specifies the time up to which the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
400 µs

17.8 Minimum I/O update time

The minimum I/O update time specifies how far the bus cycle can be reduced so that an I/O update is performed in each cycle.

Minimum I/O update time
400 µs