X20AI2632

1 General information

1.1 Other applicable documents

For additional and supplementary information, see the following documents.

Other applicable documents

Document name	Title
MAX20	X20 System user's manual
MAEMV	Installation / EMC guide

1.2 Order data

Order number	Short description	Figure
	Analog inputs	
X20AI2632	X20 analog input module, 2 inputs, ±10 V or 0 to 20 mA, 16-bit converter resolution, configurable input filter, oscilloscope functions	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O power supply connected through	
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O power supply connected through	
	Terminal blocks	
X20TB06	X20 terminal block, 6-pin, 24 VDC keyed	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 1: X20AI2632 - Order data

1.3 Module description

The module is equipped with 2 inputs with 16-bit digital converter resolution and very fast conversion time. It is possible to select between the current and voltage signal using different terminals.

This module is designed for X20 6-pin terminal blocks. If needed (e.g. for logistical reasons), the 12-pin terminal block can also be used.

Functions:

- Scaling
- Filtering
- Error monitoring
- Analysis functions

Scaling

The A/D converter data can optionally be scaled by the user to ensure the greatest possible flexibility.

Input filter

An input filter can be configured for each individual analog input.

Error monitoring

The input signal is monitored for range overshoot, synchronization errors and invalid sampling cycles. User-defined limit values can also be defined.

Analysis functions

In addition to sampling the analog input signal, the values determined can also be analyzed:

- Limit value analysis
- Recording the sampled values
- Trace

2 Technical description

2.1 Technical data

Order number	X20AI2632
Short description	
I/O module	2 analog inputs ±10 V or 0 to 20 mA
General information	
B&R ID code	0x1BA0
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using LED status indicator and software
Inputs	Yes, using LED status indicator and software
Channel type	Yes, using software
Power consumption	
Bus	0.01 W
Internal I/O	1.2 W [1)]
Additional power dissipation caused by actuators (resistive) [W]	-
Certifications	
CE	Yes
UKCA	Yes
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X
UL	cULus E115267 Industrial control equipment
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5
DNV	Temperature: **B** (0 to 55°C) Humidity: **B** (up to 100%) Vibration: **B** (4 g) EMC: **B** (bridge and open deck)
LR	ENV1
KR	Yes
ABS	Yes
BV	**EC33B** Temperature: 5 - 55°C Vibration: 4 g EMC: Bridge and open deck
EAC	Yes
KC	Yes
Analog inputs	
Input	±10 V or 0 to 20 mA, via different terminal connections
Input type	Differential input
Digital converter resolution	
Voltage	±15-bit
Current	15-bit
Conversion time	50 µs for all inputs
Output format	INT
Output format	
Voltage	INT 0x8001 - 0x7FFF / 1 LSB = 0x0001 = 305.176 µV
Current	INT 0x0000 - 0x7FFF / 1 LSB = 0x0001 = 610.352 nA
Input impedance in signal range	
Voltage	20 MΩ
Current	-
Load	
Voltage	-
Current	<400 Ω
Input protection	Protection against wiring with supply voltage
Permissible input signal	
Voltage	Max. ±30 V
Current	Max. ±50 mA
Output of digital value during overload	
Undershoot	
Voltage	0x8001
Current	0x0000
Overshoot	
Voltage	0x7FFF
Current	0x7FFF
Conversion procedure	SAR
Input filter	Hardware - Third-order low-pass filter / cutoff frequency 10 kHz

Table 2: X20AI2632 - Technical data

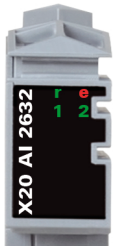
Order number	X20AI2632
Max. error	
Voltage	
Gain	0.08% 2)
Offset	0.01% 3)
Current	
Gain	0.08% 2)
Offset	0.02% 4)
Max. gain drift	
Voltage	0.01%/°C 2)
Current	0.01%/°C 2)
Max. offset drift	
Voltage	0.001%/°C 3)
Current	0.002%/°C 4)
Common-mode rejection	
DC	70 dB
50 Hz	70 dB
Common-mode range	±12 V
Crosstalk between channels	<-70 dB
Nonlinearity	
Voltage	<0.01% 3)
Current	<0.015% 4)
Insulation voltage between channel and bus	500 V_{eff}
Electrical properties	
Electrical isolation	Channel isolated from bus Channel not isolated from channel
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation elevation above sea level	
0 to 2000 m	No limitation
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
Degree of protection per EN 60529	IP20
Ambient conditions	
Temperature	
Operation	
Horizontal mounting orientation	-25 to 60°C
Vertical mounting orientation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical properties	
Note	Order 1x terminal block X20TB06 or X20TB12 separately. Order 1x bus module X20BM11 separately.
Pitch	$12.5^{+0.2}$ mm

Table 2: X20AI2632 - Technical data

1) To reduce power dissipation, B&R recommends bridging unused inputs on the terminals or configuring them as current signals.
2) Based on the current measured value.
3) Based on the 20 V measurement range.
4) Based on the 20 mA measurement range.

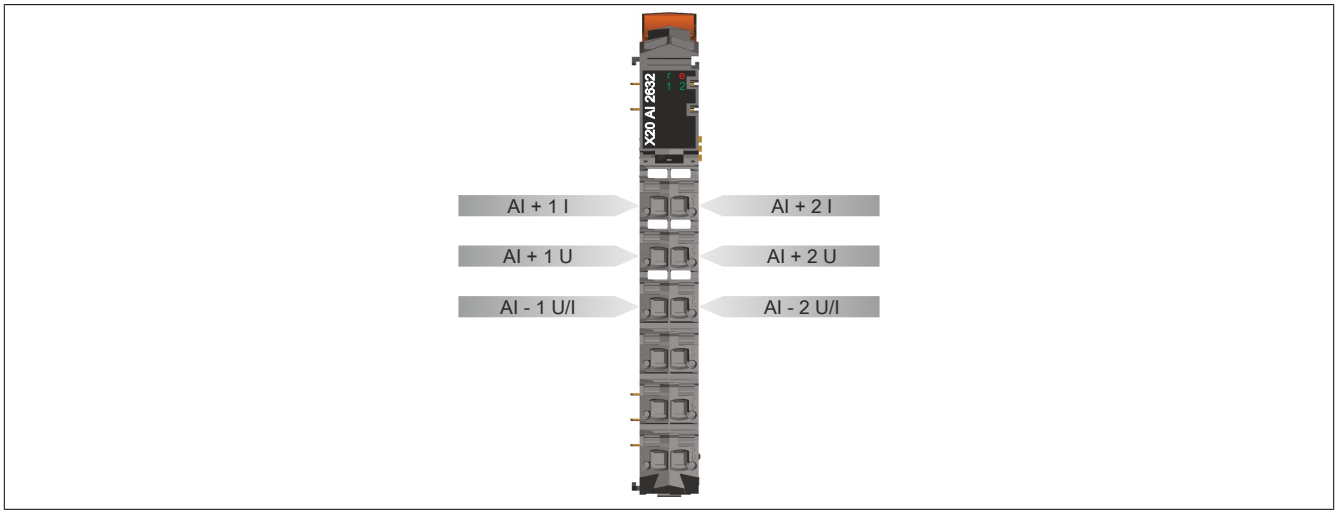
2.2 LED status indicators

For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" in the X20 System user's manual.

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
			Double flash	System error: • Violation of the scan time • Synchronization error
	1 - 2	Green	Off	Open line[2] or sensor is disconnected
			On	Analog/digital converter running, value OK

1) Depending on the configuration, a firmware update can take up to several minutes.
2) Open line detection only possible when measuring voltage.

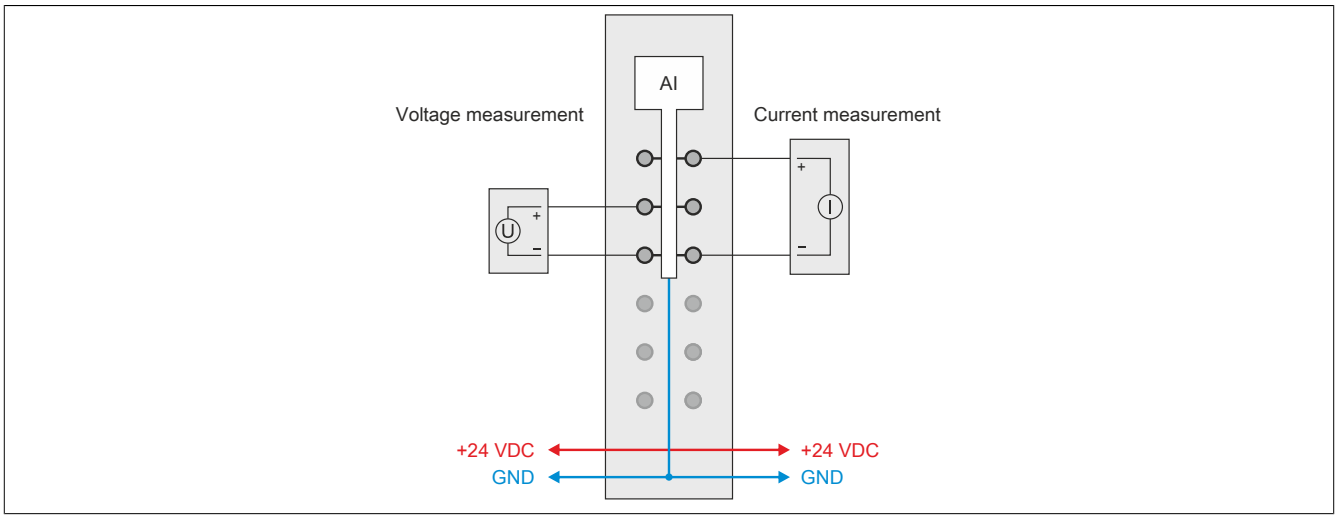
2.3 Pinout



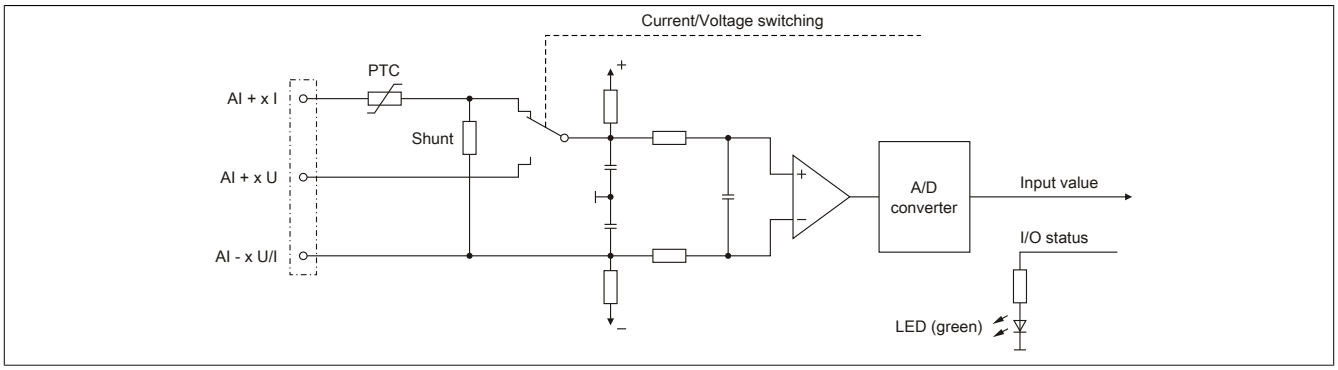
2.4 Connection example

To prevent disturbances, the following modules must be separated by at least one module:

- Bus receiver X20BR9300
- Supply module X20PS3300/X20PS3310
- Supply module X20PS9400/X20PS9402
- Power supply module X20PS9600/X20PS9602
- Controller



2.5 Input circuit diagram



3 Function description

3.1 Analog inputs

The module is equipped with analog inputs with connected 16-bit A/D converters. Each of the inputs can be configured separately for either voltage or current input for the following ranges:

- Permissible voltage: ±10 V
- Permissible current: 0 to 20 mA

Configuration must take place in addition to using suitable terminals.

> **Information:**
>
> **The register is described in "Channel configuration" on page 16.**

3.1.1 Scaling

The A/D converter data can optionally be scaled by the user. The following additional registers are available for this:

- Gain = ku
- Offset = du

Scaling calculation:

Scaled value = k * A/C value + d

Gain $k = k_{Calibration} * ku$

Offset $d = d_{Calibration} + du$

The value must be limited since it can exceed the 16-bit constraints. If the application requires a restriction of the range of values, the user can define custom limit values. These are also used for the module's error statistics.

> **Information:**
>
> **Within the module, 32-bit numbers are used for the limit values. A limit value violation can therefore also be detected if the permissible range of values of -32768 to 32767 has been defined.**

> **Information:**
>
> **The registers are described in "User-defined scaling" on page 17.**

3.1.2 Filtering

If filtering has been enabled, the basic data of the A/D converters is filtered per channel. The filter order and respective cutoff frequency of the low-pass filter can be configured for this.

Internal filter orders greater than 1 are implemented as cascaded first-order filters.

Calculating the cutoff frequency of an nth-order filter:

Cutoff frequency = Cutoff frequency$_{n}$ / ((2 ^ (1 / n) - 1) ^ 0.5)

Approximate calculation

yn = a * xn + b * y(n-1)

a = Sampling time$_{Sec}$ / (Sampling time$_{Sec}$ + 1 / (2 Pi * Cutoff frequency$_{Hz}$))

b = 1 - a

Information:

Since low-pass filtering takes place using an approximation procedure with fixed-point arithmetic, there are discrepancies to the effective cutoff frequency that depend on the sampling cycle and filter sequence.

Information:

The registers are described in "Filtering" on page 16.

3.2 Error monitoring

There are various counter registers in the module that can be used to record the occurrence of certain errors.

The counters in these registers follow the rules of the event error counter, i.e. each occurrence or reset of an error increases the counter value. The last bit of the counter indicates the error state:

- Last bit = 1 → Error pending
- Last bit = 0 → No error

The following errors are monitored:

- **Synchronization error**
  This error shows how often the conversion task was triggered more than 5 µs after the previous X2X cycle.
- **Invalid sampling cycles**
  This error indicates a cycle time violation. The error occurs if the conversion task triggers a sampling task before the last sampling cycle has been completed.
- **Workspace overshoots**
  This indicates errors outside the maximum possible measurement range of the module.
- **Range undershoots**
  This indicates range undershoots below the value set as "Minimum limit value".
- **Range overshoots**
  This indicates range overshoots above the value set as "Maximum limit value".

Overshoots and undershoots

These counters are only operated if the static error counters are enabled in the channel configuration.

Information:

The registers are described in "Error monitoring and counters" on page 18.

3.3 Analysis functions

In addition to sampling the analog input signal, this module can also be used to perform additional analysis of the values obtained.

3.3.1 Limit value analysis

Limit value analysis must be enabled for the desired channel. The sampled value of the channel is then compared with the minimum and maximum values stored internally within the module. If a new measurement period is triggered, the values from the last measuring period can be read out from the registers provided for this purpose.

If limit value analysis has been enabled for a channel, the sampled minimum and maximum values are latched within the module. A measurement period can be triggered via the control byte. If the corresponding configured edge is generated by the application, the limit values of the last measurement period are displayed and the internal latch registers are reset.

> **Information:**
>
> **The registers are described in "Limit values" on page 22.**

3.3.2 Recording the sampled values

If the recording of sampled values has been enabled for a channel, the sampled values are also recorded in a module-internal FIFO memory. When the configured event occurs, the contents of the FIFO memory are transmitted to the application.

> **Information:**
>
> **Recording of sampled values can only be used if the module is operated on an X2X master that is a type SG4 controller.**

The analog signal is sampled in 2 steps.

- **Conversion task**

  The A/D converter digitalizes the inputs signals for the enabled inputs once per conversion cycle. Then the results are available internally in the module. To ensure that this process is executed without delays, the corresponding task will be handled with very high priority.

  The timespan needed for conversion results from the set sampling time.
- **Processing task**

  The converted A/D converter values are further processed according to the user settings (filtering, scaling, limit values, error statistics, min/max analysis, hysteresis comparison). The task for this process has low priority. The timespan needed for further processing depends on the configured functions and is the second portion of the sampling time.

Cycle time violation

In normal operation, further processing is triggered after each conversion. The conversion and sampling tasks run synchronous to one another. If the predefined sampling time is not sufficient to convert all enabled channels and complete the configured functions, a cycle time violation occurs.

> **Information:**
>
> **The register is described in "Sampling time" on page 16.**

3.3.3 Trace

If the module is operated on a type SG4 controller, the digitized input values can be recorded by the module. Module monitoring must be enabled to use measured value recording.

Recording must be enabled for the desired channel. The enable bits can then control the recording at runtime. The sampled values are recorded in the module's internal FIFO memory.

If the previously defined state occurs on the channel, the contents of the FIFO memory are transmitted to the application. Whether the FIFO memory continued to be filled depends on how recording is configured.

Information:

The trace mechanism cannot be used if the module is operated behind a bus controller, but only when it is directly connected to the controller.

Information:

The registers are described in "Trace" on page 22.

Library "AsIOTrc" is used to read out the trace data.

Register "TraceChannelEnable" on page 22 determines the structure of the trace buffer.

Example of the structure of the trace buffer:

Both channels of the module are used in this example. Both channels are sampled per trigger and stored one after the other in the trace buffer.

Channel sequence
1
2
1
2
1
2
:

The length of the trace buffer is determined with registers "TraceTriggerStart" on page 26 and "TraceTriggerStop" on page 26.

Parameter "Number of trace buffers" must be defined in Automation Studio in order to configure the trace function block.

3.3.3.1 Comparator for trigger conditions

In order to adapt the trace as closely as possible to the requirements of the application, the trace function can also be controlled using the comparator. Threshold values (hysteresis) can be defined within the permitted range of values to do so. 2 status bits are then generated for each enabled channel:

- **InRange bit**
  The InRange status is "1" if the measured value falls within the defined limits.
  The InRange status is "0" if the measured value falls outside the defined limits.
- **Threshold value bit**
  The threshold value bit is "1" if the measured value exceeds the upper threshold value.
  The threshold value bit is "0" if the measured value falls below the lower threshold value.

The InRange and threshold bits of all channels are combined in the least significant byte of register CompState-Collection. In addition, the states of the previous sampling are stored in the high-order byte.

The 4 status messages of each channel can be linked via a link mask using AND or OR operators according to the following logic and used as triggers for recordings.

```
delta = (Current_HysteresisStatus ^ NominalValues)// Difference between current status and preset
cond = delta & Selected_HysteresisStatusBits// Eliminate irrelevant status messages
cond = Selected_HysteresisStatusBits (Current_HysteresisStatus ^ NominalValues)
if((0==(cond & ~LogicalOperators)) &&
(0!=(~cond & LogicalOperators))) {=> Generate trigger event}
```

	Corresponds to register:
Selected_HysteresisStatusBits	cfgComp_EnableMask
Current_HysteresisStatus	CompStateCollection
Nominal values	cfgComp_NominalState
Logical operators	cfgComp_ConditionTypeMask

Information:

The registers are described in "Comparator for trigger conditions" on page 24.

3.3.3.2 Recording measured values

The module has 16 kB available for the trace. The limitation of the FIFO memory means that a maximum of 8192 analog values can be recorded. The memory is divided evenly between the enabled channels. The actual maximum number of possible recordings therefore depends on the number of channels registered for the trace:

1 channel enabled: Maximum 8192 recordings
2 channels enabled: Maximum 4096 recordings per channel

Time-shifted recording

If the recording should be defined with a time offset to the trigger, additional conditions can be defined for shifting the start and stop time.

Information:

The registers are described in "Time-offset trace" on page 26.

4 Commissioning

4.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use other registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" in the X20 user's manual (version 3.50 or later).

4.1.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN I/O.

5 Register description

5.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" in the X20 System user's manual.

5.2 Function model 0 - default

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration - Frame size						
-	AsynSize	-				
Configuration						
257	ConfigOutput01 (channel configuration)	USINT				•
289	ConfigOutput06 (channel configuration)	USINT				•
	Sampling time					
390	ConfigOutput24 (sampling time)	UINT				•
	Filtering					
259	ConfigOutput26 (filter order)	USINT				•
291	ConfigOutput28 (filter order)	USINT				•
262	ConfigOutput27 (filter cutoff frequency)	UINT				•
294	ConfigOutput29 (filter cutoff frequency)	UINT				•
	Scaling					
276	ConfigOutput04 (user-defined gain)	DINT				•
308	ConfigOutput09 (user-defined gain)	DINT				•
284	ConfigOutput05 (user-defined offset)	DINT				•
316	ConfigOutput10 (user-defined offset)	DINT				•
	User-defined limit values					
266	ConfigOutput02 (minimum limit value)	UINT				•
298	ConfigOutput07 (minimum limit value)	UINT				•
270	ConfigOutput03 (maximum limit value)	UINT				•
302	ConfigOutput08 (maximum limit value)	UINT				•
Communication						
0	AnalogInput01	INT	•			
4	AnalogInput02	INT	•			
650	SampleCycleCounter	UINT		•		
	Error monitoring and counters					
641	Channel status	USINT	•			
	Channel01OK	Bit 0				
	Channel02OK	Bit 1				
	SyncStatus	Bit 6				
	ConvertionCycle	Bit 7				
654	SampleCycleViolationErrorCounter	UINT		•		
658	SynchronizationViolationErrorCounter	UINT		•		
2097	Range undershoot and overshoot	USINT	•			
	Channel01underflow	Bit 0				
	Channel02underflow	Bit 1				
	Channel01overflow	Bit 4				
	Channel02overflow	Bit 5				
2099	Workspace overshoot	USINT	•			
	Channel01outofrange	Bit 0				
	Channel02outofrange	Bit 1				
518	Ch01OutOfRange	UINT		•		
550	Ch02OutOfRange	UINT		•		
522	Ch01Underflow	UINT		•		
554	Ch02Underflow	UINT		•		
526	Ch01Overflow	UINT		•		
558	Ch02Overflow	UINT		•		
Additional analysis functions						
133	ConfigOutput21 (trigger condition on falling edge)	USINT				•
135	ConfigOutput22 (trigger condition on rising edge)	USINT				•
129	Analysis control byte	USINT			•	
	TraceTrigger01	Bit 0				
	MinMaxStart01	Bit 4				
	MinMaxStart02	Bit 5				
129	Analysis status byte	USINT	•			
	MinMaxStart01Readback	Bit 4				
	MinMaxStart02Readback	Bit 5				
	Limit values					
530	MinInput01	INT	•			

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
562	MinInput02	INT	•			
534	MaxInput01	INT	•			
566	MaxInput02	INT	•			
538	Ch01MinMaxLatchCounter	UINT		•		
570	Ch02MinMaxLatchCounter	UINT		•		
	Trace configuration					
1026	TraceChannelEnable	USINT				•
1030	TraceSampleDepth	UINT				•
4157	ConfigOutput25 (trace priority)	USINT				•
1037	Enabling the trace function	USINT			•	
	TraceEnable01	Bit 0				
1089	Trace status	USINT	•			
	TraceEnabled	Bit 0				
	TraceWriteActive	Bit 2				
	TraceReadActive	Bit 3				
	ReadyForTrigger	Bit 4				
	TriggerActive	Bit 5				
	TraceOK	Bit 6				
	TraceError	Bit 7				
1094	FreeBufferSize	UINT	•			
1098	TriggerCount	UINT	•			
1102	TriggerFailCount	UINT	•			
	Comparator					
450	cfgComp_LowLimitCh01	INT			(•)	•
458	cfgComp_LowLimitCh02	INT			(•)	•
454	cfgComp_HighLimitCh01	INT			(•)	•
462	cfgComp_HighLimitCh02	INT			(•)	•
662	CompStateCollection	UINT	•			
490	cfgComp_NominalState	UINT				•
482	cfgComp_EnableMask	UINT				•
486	cfgComp_ConditionTypeMask	UINT				•
	Time-offset trace					
1042	TraceTriggerStart	INT				•
1046	TraceTriggerStop	UINT				•

5.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration - Frame size							
-	-	AsynSize	-				
Configuration							
257	-	ConfigOutput01 (channel configuration)	USINT				•
289	-	ConfigOutput06 (channel configuration)	USINT				•
	Sampling time						
390	-	ConfigOutput24 (sampling time)	UINT				•
	Filtering						
259	-	ConfigOutput26 (filter order)	USINT				•
291	-	ConfigOutput28 (filter order)	USINT				•
262	-	ConfigOutput27 (filter cutoff frequency)	UINT				•
294	-	ConfigOutput29 (filter cutoff frequency)	UINT				•
	Scaling						
276	-	ConfigOutput04 (user-defined gain)	DINT				•
308	-	ConfigOutput09 (user-defined gain)	DINT				•
284	-	ConfigOutput05 (user-defined offset)	DINT				•
316	-	ConfigOutput10 (user-defined offset)	DINT				•
	User-defined limit values						
266	-	ConfigOutput02 (minimum limit value)	UINT				•
298	-	ConfigOutput07 (minimum limit value)	UINT				•
270	-	ConfigOutput03 (maximum limit value)	UINT				•
302	-	ConfigOutput08 (maximum limit value)	UINT				•
Communication							
0	0	AnalogInput01	INT	•			
4	2	AnalogInput02	INT	•			
650	-	SampleCycleCounter	UINT		•		
	Error monitoring and counters						
641	-	Channel status	USINT		•		
		Channel01OK	Bit 0				
		Channel02OK	Bit 1				
		SyncStatus	Bit 6				
		ConvertionCycle	Bit 7				
654	-	SampleCycleViolationErrorCounter	UINT		•		
658	-	SynchronizationViolationErrorCounter	UINT		•		
2097	-	Range undershoot and overshoot	USINT		•		
		Channel01underflow	Bit 0				
		Channel02underflow	Bit 1				
		Channel01overflow	Bit 4				
		Channel02overflow	Bit 5				
2099	-	Workspace overshoot	USINT		•		
		Channel01outofrange	Bit 0				
		Channel02outofrange	Bit 1				
518	-	Ch01OutOfRange	UINT		•		
550	-	Ch02OutOfRange	UINT		•		
522	-	Ch01Underflow	UINT		•		
554	-	Ch02Underflow	UINT		•		
526	-	Ch01Overflow	UINT		•		
558	-	Ch02Overflow	UINT		•		
Additional analysis functions							
133	-	ConfigOutput21 (trigger condition on falling edge)	USINT				•
135	-	ConfigOutput22 (trigger condition on rising edge)	USINT				•
129	-	Analysis control byte	USINT				•
		TraceTrigger01	Bit 0				
		MinMaxStart01	Bit 4				
		MinMaxStart02	Bit 5				
129	-	Analysis status byte	USINT		•		
		MinMaxStart01Readback	Bit 4				
		MinMaxStart02Readback	Bit 5				
	Limit values						
530	-	MinInput01	INT		•		
562	-	MinInput02	INT		•		
534	-	MaxInput01	INT		•		
566	-	MaxInput02	INT		•		
538	-	Ch01MinMaxLatchCounter	UINT		•		
570	-	Ch02MinMaxLatchCounter	UINT		•		

1) The offset specifies the position of the register within the CAN object.

5.4 Configuration

5.4.1 Channel configuration

Name:
ConfigOutput01 for channel 1
ConfigOutput06 for channel 2

The individual inputs for processing the current or voltage signal are configured in these registers. This configuration must be made in addition to using suitable terminals.

Filtering, analysis and error monitoring (bits 4 to 6) can only be used if the channel is enabled (bit 7 = 0).

Data type	Values	Bus controller default setting
USINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0	Terminal selector	0	Voltage terminal for ±10 VDC (bus controller default setting)
		1	Current terminal for 0 to 20 mA
1	Gain selector	0	Voltage ±10 VDC (bus controller default setting)
		1	Current 0 to 20 mA
2 - 3	Reserved	-	
4	Filtering active	0	Inactive (bus controller default setting)
		1	Active
5	Minimum/Maximum analysis active	0	Inactive (bus controller default setting)
		1	Active
6	Error monitoring active	0	Inactive (bus controller default setting)
		1	Active
7	Enables channel	0	Channel enabled (bus controller default setting)
		1	Channel disabled

5.4.2 Sampling time

Name:
ConfigOutput24

The sampling time is set to µs in this register. This makes it possible to improve the sampling cycle (resolution = 1 µs). The lowest configurable cycle time is 50 µs.

Data type	Value	Information
UINT	50 to 10,000	Bus controller default setting: 100

Information:

Values that are too low for the cycle time will result in cycle time violations.

5.4.3 Filtering

5.4.3.1 Filter order

Name:
ConfigOutput26 for channel 1
ConfigOutput28 for channel 2

The filter order is specified in this register. The "Filter cutoff frequency" on page 17 register is used to configure the respective cutoff frequency of the filter.

Data type	Value	Information
USINT	1 to 4	Bus controller default setting: 0

5.4.3.2 Filter cutoff frequency

Name:
ConfigOutput27 for channel 1
ConfigOutput29 for channel 2

The cutoff frequency of the respective filter is configured in these registers.

Data type	Value	Information
UINT	1 to 65,535	Cutoff frequency in hertz. Bus controller default setting: 0

Information:

The highest cutoff frequency is limited by the Nyquist Shannon sampling theorem (based on the sampling cycle time). The system does not check for violations of this sampling theorem.

5.4.4 User-defined scaling

5.4.4.1 User-defined gain

Name:
ConfigOutput04 for channel 1
ConfigOutput09 for channel 2

The user-defined gain for the A/D converter data of the respective physical channel can be specified in these registers.

The value 65536 (0x10000) corresponds to a gain of 1.

Data type	Values	Information
DINT	-2,147,483,648 to 2,147,483,647	Bus controller default setting: 65536

5.4.4.2 User-defined offset

Name:
ConfigOutput05 for channel 1
ConfigOutput10 for channel 2

The user-defined offset for the A/D converter data of the respective physical channel can be specified in this register.

The value 65536 (0x10000) corresponds to an offset of 1.

Data type	Values	Information
DINT	-2,147,483,648 to 2,147,483,647	Bus controller default setting: 0

5.4.5 User-defined limit values

5.4.5.1 Minimum limit value

Name:
ConfigOutput02 for channel 1
ConfigOutput07 for channel 2

The minimum limit value is configured in this register. This limit value is also used for the undershoot error statistics (see register "Ch0xUnderflow" on page 20).

Data type	Values	Information
INT	-32768 to 32767	Bus controller default setting: -32768

5.4.5.2 Maximum limit value

Name:
ConfigOutput03 for channel 1
ConfigOutput08 for channel 2

The maximum limit value is configured in this register. This limit value is also used for the overflow error statistics (see register "Ch0xOverflow" on page 20).

Data type	Values	Information
INT	-32767 to 32767	Bus controller default setting: 32767

5.5 Communication - General

The analog inputs of the module convert the current or voltage values with a resolution of 16 bits. The information can be used by the application via the registers described here.

5.5.1 Analog inputs

Name:
AnalogInput01 to AnalogInput02

The analog input value is mapped in this register depending on the configured operating mode.

Data type	Value	Input signal
INT	-32,768 to 32,767	Voltage signal ±10 VDC
	0 to 32,767	Current signal 0 to 20 mA

5.5.2 Sampling cycle counter

Name:
SampleCycleCounter

The number of times the input signal has been sampled is provided in this register.

Data type	Values
UINT	0 to 65535

5.6 Error monitoring and counters

5.6.1 Channel status

Name:
Channel01OK to Channel02OK
SyncStatus
ConvertionCycle

This register collects error messages synchronously with the network cycle. Temporary error states that were registered in a conversion cycle remain active for at least 2 network cycles. In order to receive detailed error information, the corresponding error counters and X2X network events should also be observed.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel01OK	0	OK
		1	Errors
1	Channel02OK	0	OK
		1	Errors
2 - 5	Reserved	-	
6	SyncStatus[1)]	0	OK
		1	Not synchronized
7	ConvertionCycle[2)]	0	OK
		1	Errors

1) Identical to bit 0 of the registers "SynchronizationViolationErrorCounter" on page 19.
2) Identical to bit 0 of the registers "SampleCycleViolationErrorCounter" on page 19.

5.6.2 Workspace overshoot

Name:
Channel01outofrange to Channel02outofrange

This register indicates whether the input value overshoots the module's maximum measurement range. The individual bits in this register are identical to the value of the lowest bit of register "Ch0xOutOfRange" on page 20.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel01outofrange	0	No error
		1	Working range violation (pos.) of channel 1
1	Channel02outofrange	0	No error
		1	Working range violation (pos.) of channel 2
2 - 7	Reserved	-	

5.6.3 Range undershoot and overshoot

Name:
Channel01underflow to Channel02underflow
Channel01overflow to Channel02overflow

This register indicates whether the limit values defined by registers "Minimum limit value" on page 17 and "Maximum limit value" on page 17 have been overshot or undershot. The individual bits in this register are identical to the value of the lowest bit of registers "Ch0xUnderflow" on page 20 and "Ch0xOverflow" on page 20.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel01underflow	0	No error
		1	Range exceeded (.neg) on channel 1
1	Channel02underflow	0	No error
		1	Range exceeded (.neg) on channel 2
2 - 3	Reserved	-	
4	Channel01overflow	0	No error
		1	Range exceeded (.pos) on channel 1
5	Channel02overflow	0	No error
		1	Range exceeded (.pos) on channel 2
6 - 7	Reserved	-	

5.6.4 Counter for synchronization errors

Name:
SynchronizationViolationErrorCounter

This register counts how often the conversion task was triggered more than 5 µs after the next-coming X2X cycle. In this case, the module is considered being no longer synchronized with X2X Link.

Data type	Value	Information[1)]
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

1) For details, see "Error monitoring" on page 8.

5.6.5 Counter for faulty sampling cycles

Name:
SampleCycleViolationErrorCounter

This register is used to indicate the number of cycle time violations that have occurred thus far. A cycle time violation occurs if the conversion tasks initiates a sampling task before the last sampling cycle has finished. See "Recording the sampled values" on page 9.

Data type	Value	Information[1)]
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

1) For details, see "Error monitoring" on page 8.

5.6.6 Counter for workspace overshoots

Name:
Ch01OutOfRange to Ch02OutOfRange

This register indicates errors outside the maximum possible measurement range of the module. These errors result in a final deflection of the A/D converter.

Data type	Value	Information[1)]
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

1) For details, see "Error monitoring" on page 8.

5.6.7 Counter for range exceeded violations (neg.)

Name:
Ch01Underflow to Ch02Underflow

This register indicates the range undershoots below the value set in register "Minimum limit value" on page 17.

Data type	Value	Information[1)]
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

1) For details, see "Error monitoring" on page 8.

5.6.8 Counter for range exceeded violations (pos.)

Name:
Ch01Overflow to Ch02Overflow

This register indicates the range overshoots above the value set in register "Maximum limit value" on page 17.

Data type	Value	Information[1)]
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

1) For details, see "Error monitoring" on page 8.

5.7 Analysis functions

In addition to sampling the analog input signal, this module can also be used to perform additional analysis of the values obtained.

5.7.1 Trigger condition on falling edge

Name:
ConfigOutput21

This register can be used to configure whether the falling edge is used to trigger the trace and determine the input value in register "Analysis control byte" on page 21.

Data type	Values	Bus controller default setting
USINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0	TraceTrigger01	0	No trigger (bus controller default setting)
		1	Falling edge active as trigger
1 - 3	Reserved	-	
4	MinMaxStart01	0	No determination (bus controller default setting)
		1	Falling edge determines input value of channel 1
5	MinMaxStart02	0	No determination (bus controller default setting)
		1	Falling edge determines input value of channel 2
6 - 7	Reserved	0	

5.7.2 Trigger condition on rising edge

Name:
ConfigOutput22

This register can be used to configure whether the rising edge is used to trigger the trace and determine the input value in register "Analysis control byte" on page 21.

Data type	Values	Bus controller default setting
USINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0	TraceTrigger01	0	Trigger not initiated on positive edge (bus controller default setting)
		1	Rising edge active as trigger
1 - 3	Reserved	-	
4	MinMaxStart01	0	No determination (bus controller default setting)
		1	Rising edge determines input value of channel 1
5	MinMaxStart02	0	No determination (bus controller default setting)
		1	A positive edge determines the input value of channel 2.
6 - 7	Reserved	0	

5.7.3 Analysis control byte

Name:
TraceTrigger01
MinMaxStart01 to MinMaxStart02

The trace function and determination of the minimum/maximum input values can be started in this register. Whether the rising and/or falling edge is used to trigger the functions can be configured using the registers "Trigger condition on falling edge" on page 20 and "Trigger condition on rising edge" on page 21.

Data type	Values	Bus controller default setting
USINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0	TraceTrigger01	0	Trigger/Trace not triggered (bus controller default setting)
		1	Initiates trigger/trace
1 - 3	Reserved	-	
4	MinMaxStart01	0	Determination not triggered (bus controller default setting)
		1	Determination of the input value of channel 1 is triggered.
5	MinMaxStart02	0	Determination not triggered (bus controller default setting)
		1	Determination of the input value of channel 2 is triggered.
6 - 7	Reserved	-	

Information:

To reduce the cyclic data transfer, this register combines the trace and limit value determination functions.

5.7.4 Analysis status byte

Name:
MinMaxStart01Readback to MinMaxStart02Readback

The currently requested module-internal analyses can be checked in this register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Reserved	-	
4	MinMaxStart01Readback	0 or 1	Current state of the trigger bits for determining the limit values on channel 1
5	MinMaxStart02Readback	0 or 1	Current state of the trigger bits for determining the limit values on channel 2
6 - 7	Reserved	-	

5.8 Limit values

5.8.1 Minimum input values

Name:
MinInput01 to MinInput02

The minimum value of the preceding trigger period is saved in this register based on the filtered, scaled and user-defined limit values. The register value is 0 if the channel is inactive.

Data type	Value
INT	-32,768 to 32,767

5.8.2 Maximum input values

Name:
MaxInput01 to MaxInput02

The maximum value of the preceding trigger period is saved in this register based on the filtered, scaled and user-defined limit values. The register value is 0 if the channel is inactive.

Data type	Value
INT	-32,768 to 32,767

5.8.3 Limit value trigger counter

Name:
Ch01MinMaxLatchCounter to Ch02MinMaxLatchCounter

The number of valid events that trigger a new measurement period for the limit value analysis is counted in this register.

Data type	Value
UINT	0 to 65535

5.9 Trace

5.9.1 Enabling channels

Name:
TraceChannelEnable

The respective channel is enabled for the trace with this register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel 1	0	Channel disabled
		1	Channel enabled
1	Channel 2	0	Channel disabled
		1	Channel enabled
2 - 7	Reserved	-	

5.9.2 Trace FIFO configuration

Name:
TraceSampleDepth

The module has 16 kB available for the trace. The limitation of the FIFO memory means that a maximum of 8192 analog values can be recorded. The memory is divided evenly between the enabled channels. The actual maximum number of possible recordings therefore depends on the number of channels registered for the trace.

Data type	Value
UINT	2 to 8192

5.9.3 Trace priority

Name:
ConfigOutput25

The priority of the trace can be increased with this register.

Data type	Value	Function
USINT	3	Standard
	6	Trace priority higher than X2X Link communication

5.9.4 Enabling the trace function

Name:

TraceEnable01

This register can be used to enable recording according to the edge control or comparator specifications.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	TraceEnable01	0	Disables the trace function
		1	Enables the trace function
1 - 7	Reserved	-	

5.9.5 Trace status

Name:
TraceEnabled
TraceWriteActive
TraceReadActive
ReadyForTrigger
TriggerActive
TraceOk
TraceError

The status of the trace is represented in this register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	TraceEnabled	0	Trace inactive
		1	Trace active
1	Reserved	-	
2	TraceWriteActive	0	Data not recorded
		1	Data recorded
3	TraceReadActive	0	Data not output/read
		1	Data output/read
4	ReadyForTrigger	0	Not ready for triggering
		1	Ready for triggering
5	TriggerActive	0	No trigger active or already executed
		1	Trigger active
6	TraceOk	0	Overflow or inactive
		1	No overflow
7	TraceError	0	No error or inactive
		1	Trace buffer full

5.9.6 Free trace buffer

Name:
FreeBufferSize

Specifies the free FIFO memory area for the trace in bytes.

Data type	Values
UINT	0 to 65535

5.9.7 Counter for trigger events

Name:
TriggerCount

This register indicates the number of trigger events that have occurred since the start of the recording.

Data type	Values
UINT	0 to 65535

5.9.8 Counter for invalid trigger events

Name:
TriggerFailCount

Counts the trigger events for which the trace could not be carried out.

Data type	Values
UINT	0 to 65535

5.9.9 Comparator for trigger conditions

5.9.9.1 Lower limit value for hysteresis

Name:
cfgComp_LowLimitCh01 to cfgComp_LowLimitCh02

The lower limit value for hysteresis is configured in this register.

Data type	Values
INT	-32768 to 32767

5.9.9.2 Upper limit value for hysteresis

Name:
cfgComp_HighLimitCh01 to cfgComp_HighLimitCh02

The upper limit value for hysteresis is configured in this register.

Data type	Values
INT	-32768 to 32767

5.9.9.3 Hysteresis status of the channels

Name:
CompStateCollection

The hysteresis status of the input channels for the current and last cycle are represented in this register.

Data type	Values
UINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel01 hysteresis status in the current cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
1	Channel01 InRange status in the current cycle	0	Value lies outside of range defined by the limit values
		1	Value is between the lower and upper limit value.
2	Channel02 hysteresis status in the current cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
3	Channel02 InRange status in the current cycle	0	Value lies outside of range defined by the limit values
		1	Value is between the lower and upper limit value.
4 - 7	Reserved	-	
8	Channel01 hysteresis status in the last cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
9	Channel01 InRange status in the last cycle	0	Value lies outside of range defined by the limit values
		1	Value is between the lower and upper limit value.
10	Channel02 hysteresis status in the last cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
11	Channel02 InRange status in the last cycle	0	Value lies outside of range defined by the limit values
		1	Value is between the lower and upper limit value.
12 - 15	Reserved	-	

5.9.9.4 Comparison state of the channels

Name:
cfgComp_NominalState

The desired comparison state for the hysteresis status is indicated in this register.

Data type	Values
UINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel01 hysteresis status in the current cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
1	Channel01 InRange status in the current cycle	0	Value lies outside of range defined by the limit values
		1	Value is between the lower and upper limit value.
2	Channel02 hysteresis status in the current cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
3	Channel02 InRange status in the current cycle	0	Value lies outside of range defined by the limit values
		1	Value is between the lower and upper limit value.
4 - 7	Reserved	-	
8	Channel01 hysteresis status in the last cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
9	Channel01 InRange status in the last cycle	0	Value lies outside of range defined by the limit values
		1	Value is between the lower and upper limit value.
10	Channel02 hysteresis status in the last cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
11	Channel02 InRange status in the last cycle	0	Value lies outside of range defined by the limit values
		1	Value is between the lower and upper limit value.
12 - 15	Reserved	-	

Information:

This is a positive list. This means that recording starts as soon as the current status message assumes the state specified here.

Whether one match is sufficient or whether several matches are required depends on the selection of the relevant hysteresis status bits and logical operators.

5.9.9.5 Selecting the relevant hysteresis status bits

Name:
cfgComp_EnableMask

This register can be used to select which status bits of the hysteresis comparison should be used to generate the trigger.

For more information about using this register, see "Comparator for trigger conditions" on page 11.

Data type	Values
UINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel01 hysteresis status in the current cycle	0	Do not use
		1	Use for generation
1	Channel01 InRange status in the current cycle	0	Do not use
		1	Use for generation
2	Channel02 hysteresis status in the current cycle	0	Do not use
		1	Use for generation
3	Channel02 InRange status in the current cycle	0	Do not use
		1	Use for generation
4 - 7	Reserved	-	
8	Channel01 hysteresis status in the last cycle	0	Do not use
		1	Use for generation
9	Channel01 InRange status in the last cycle	0	Do not use
		1	Use for generation
10	Channel02 hysteresis status in the last cycle	0	Do not use
		1	Use for generation
11	Channel02 InRange status in the last cycle	0	Do not use
		1	Use for generation
12 - 15	Reserved	-	

5.9.9.6 Logical connective operators for hysteresis status bits

Name:
cfgComp_ConditionTypeMask

This register is used to select the desired operators of the states with which the status bits are linked with one another to generate a trigger.

At least one OR operation must be configured, but it does not necessarily have to be located on a channel configured with "1" in the "cfgComp_EnableMask" on page 25 register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel01 hysteresis status in the current cycle	0	Use AND operation
		1	Use OR operation
1	Channel01 InRange status in the current cycle	0	Use AND operation
		1	Use OR operation
2	Channel02 hysteresis status in the current cycle	0	Use AND operation
		1	Use OR operation
3	Channel02 InRange status in the current cycle	0	Use AND operation
		1	Use OR operation
4 - 7	Reserved	-	
8	Channel01 hysteresis status in the last cycle	0	Use AND operation
		1	Use OR operation
9	Channel01 InRange status in the last cycle	0	Use AND operation
		1	Use OR operation
10	Channel02 hysteresis status in the last cycle	0	Use AND operation
		1	Use OR operation
11	Channel02 InRange status in the last cycle	0	Use AND operation
		1	Use OR operation
12 - 15	Reserved	-	

5.9.10 Time-offset trace

5.9.10.1 Starting the trace

Name:
TraceTriggerStart

The relative start position in relation to the configured trigger condition (pos./neg. edge) is defined in this register. Positive values mean that recording begins x samplings after the trigger condition. Negative values mean that the recording starts x samplings before the trigger condition.

With value -32768, recording is started immediately when the trace is enabled.

Data type	Value	Information
INT	-32767 to 32767	
	-32768	Continuous trace without a stopping point

5.9.10.2 Stopping the trace

Name:
TraceTriggerStop

The relative unsigned stop position in relation to the configured trigger condition is defined in this register.

- When configuring an early recording start, this value refers to the trigger event.
- When configuring a delayed start of recording, the value refers to the start of recording.

Data type	Values
UINT	0 to 65535

5.10 Acyclic frame size

Name:
AsynSize

When using the stream, the data is exchanged internally between the module and controller. A defined number of acyclic bytes is reserved for this slot for this purpose.
Increasing the acyclic frame size results in increased data throughput on this slot.

Information:

This configuration involves a driver setting that cannot be changed during runtime!

Data type	Values	Information
-	8 to 28	Acyclic frame size in bytes. Default = 24

5.11 Minimum cycle time

The minimum cycle time specifies how far the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

	Minimum cycle time
Standard priority	200 µs
High priority with trace function	300 µs

5.12 Minimum I/O update time

There is no limitation or dependency on the bus cycle time.

The I/O update time is defined using the "Sampling time" register. The fastest possible sampling time depends on the number of channels to be converted and the configuration.